DC-50 GHz Low Loss Switch Matrix Design in High Resistivity Trap-Rich SOI

Bo Yu[1], Kaixue Ma[2], Fanyi Meng[1], Thangarasu Bharatha Kumar[3], and Kiat Seng Yeo[3]

[1]School of EEE, Nanyang Technological University, Singapore

[2]School of Physical Electronics, University of Electronic Science and Technology of China, Chengdu, China

[3]Singapore University of Technology and Design, Singapore

yubo0002@e.ntu.edu.sg

***Abstract*—This paper presents low insertion loss, high isolation, ultra wideband (DC to 50 GHz) 2 x 2 switch matrix in a 300mm 0.13 µm high substrate resistivity trap-rich SOI. The switches are designed by using a series-shunt-series configuration with input and output matching networks. The designed switches achieve a 1.8 dB of low insertion loss and a high isolation of 38 dB up to 50 GHz. 1dB-compression point of designed switches are larger than 19 dBm from DC to 50 GHz. The active chip area of designed 2 x 2 switch matrix is only 0.28 x 0.21 mm^2.**

***Keywords*—Switch matrix, ultra wideband, SOI**

I. Introduction

RF switch matrix is widely used in modern communication systems such as wireless internet, relay stations and satellite communications, etc., which need route RF signals between multiple inputs and multiple outputs. The ability of switches to operate over wide bandwidth is becoming increasingly important to enable wideband or multi-band systems on chip. Design high performance switch matrix including lower insertion loss, higher isolation and power handling capability over an ultra-wide bandwidth from DC to cross millimeter-wave boundary still remains quite challenging.

RF switch matrixes have been designed by various processes and technology nodes previously, including GaAs JFET [1], 0.5 µm pHEMT process [2], PIN diode [3], 0.13 µm CMOS [4], etc. However, all these designs are limited within DC to 12 GHz frequency range.

In recent years, by using high resistivity (HR) substrate, silicon-on–insulator (SOI) technology has been adopted for ultra wideband RF switch design [5], thanks to SOI reduced parasitic capacitance and substrate loss. However, HR SOI still suffers from parasitic surface conduction due to fixed charges within the buried oxide (BOX) layer which attract free carriers near the Si/SiO$_2$ interface and will reduce the substrate effective resistivity and increase substrate losses. To introduce an additional trap-rich (TR) layer, which can capture the free carriers is an efficient solution to drastically reduce the crosstalk.

In this work, we present 0.13 µm HR TR SOI based 2 x 2 double-pole-double-throw (DPDT) switch design, the designed switches achieve the low insertion loss / high isolation of 1.2 dB / 37 dB from DC to 30 GHz and 1.8 dB / 38 dB from DC to 50 GHz, respectively.

II. Wideband DPDT SOI Switch Design

A. Configulation

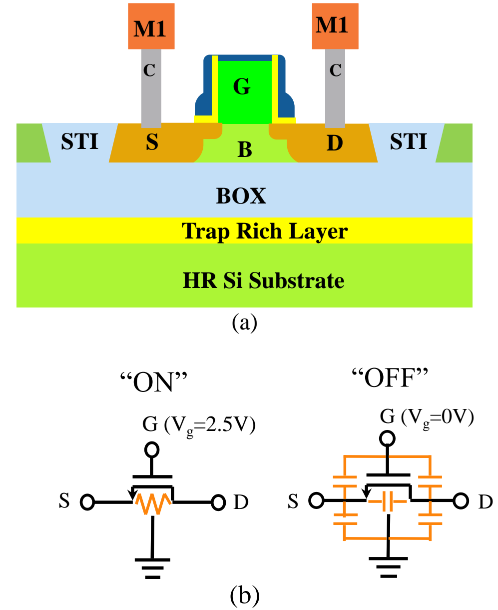

Fig.1. (a) Cross sectional view of an SOI NMOS and (b) Small signal model of SOI MOSFET in "ON" state and "OFF" state.

Globalfoundries' 0.13-µm RFSOI process offers 2.5 V body-tied thick gate oxide NMOS switch transistor (nominal gate length, L_g = 0.2 µm), with a low R_{on}*C_{off} product, the oxide thickness is about 6.5 nm. The schematic of high resistivity trap-rich SOI substrate and simplified model of the SOI NMOS are shown in Fig. 1. The thickness of the top silicon and BOX are around 1600 Å and 2000 Å, respectively, the handle silicon (Si) substrate has a resistivity larger than 3000 Ω-cm, the trap rich layer is in between the BOX and handle Si.

2.5 V body-tied SOI NMOS, with nominal channel length, L_g = 0.2 µm, is used for switch design, the designed DPDT

switches are based on series-shunt-series with input and output matching network topology to achieve a wideband operation.

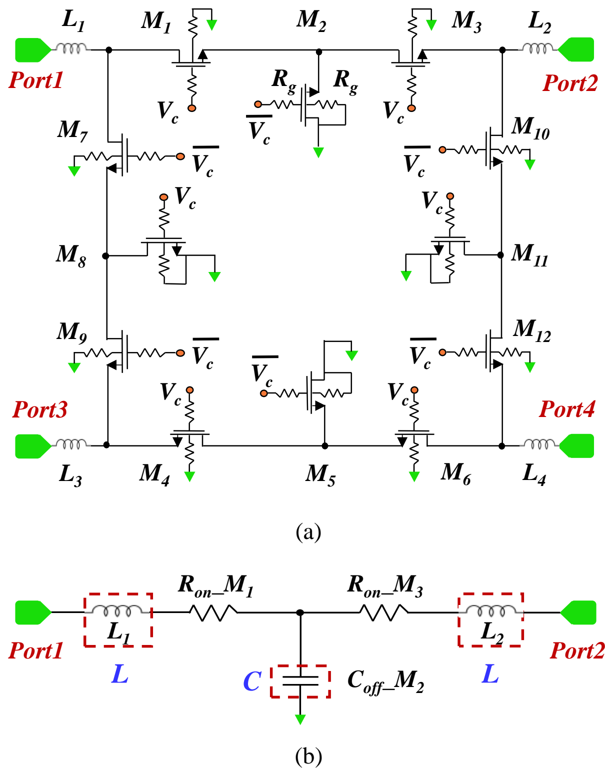

Fig. 2. (a) Schematic of the DPDT switch, and (b) equivalent *L-C-L* T-matching network model

On-chip series inductors are used and act as *L-C-L* T-matching circuit using the off-state capacitance of the shunt NMOS as shunt capacitor *C*. The final topology for DPDT switch and equivalent *L-C-L* T-matching network model are shown in Fig. 2. The DPDT switch is constructed by four symmetric single-pole single-throw (SPST) switch branches in a ring-type structure. One SPST branch, with series transistors M_1 and M_3, and shunt transistor M_2, forms the path between Port1 and Port2, and the other three SPST branches, which also combined by series-shunt-series transistors, forms other paths between Port1 and Port3, Port2 and Port4, and Port3 and Port4, respectively. The L_1, L_2, L_3, and L_4 are used as the matching inductors for each branch. When V_C is high (= 3.3 V), series transistor M_1, M_3, M_4, M_6, and shunt transistor, M_8 and M_{11}, are turned on, at the same time, series transistor M_7, M_9, M_{10}, M_{12}, and shunt transistor, M_2 and M_5, are turned off, so RF signal can flow between Port1 and Port2, and between Port3 and Port4, while cannot flow between Port1 and Port3, and between Port2 and Port4. On the contrary, when V_C is low (-3.3 V), RF signal can only be transferred between Port1 and Port3, and between Port2 and Port4. In this work, two groups of series-shunt-series transistors are designed for evaluation. DPDT1 is designed with series-shunt-series transistor widths = 75 µm/100 µm/75 µm, and $L_1 = L_2 = L_3 = L_4 = 140$ pH, DPDT2 is designed with series-shunt-series transistor widths = 150 µm/100 µm/150 µm, and $L_1 = L_2 = L_3 = L_4 = 170$ pH. External resistors, R_g = 20 kΩ are connected to gate and body of each transistor for ac floating to prevent signal leakage and gate oxide breakdown.

This DPDT switch only occupies a small chip area of 0.28 x 0.21 mm^2. Same DPDT layout but with shorter channel length (L_g = 0.13 µm) is also designed to investigate the channel length effect on ultra wideband switch performance.

III. Simulation Result

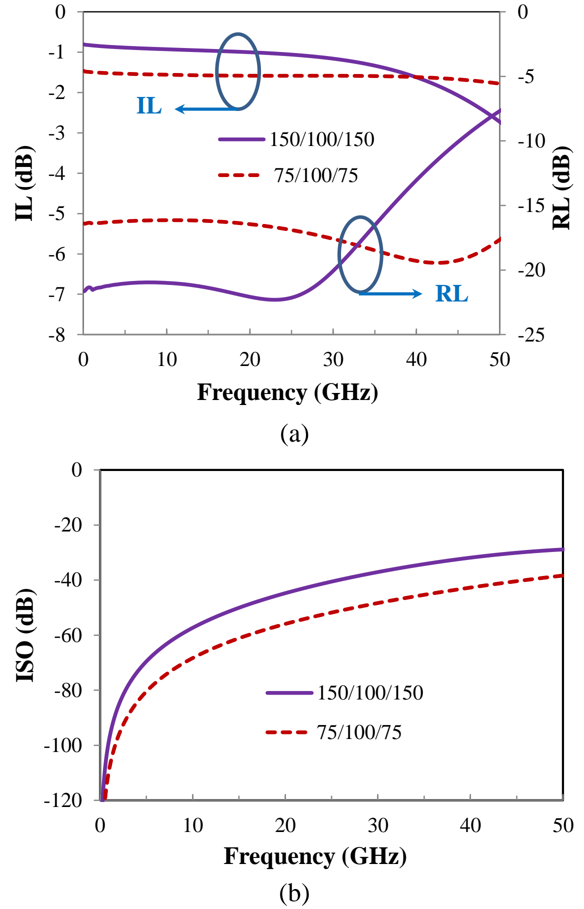

Fig. 3. Simulated S-parameters for designed DPDT switches, (a) Insertion loss (IL) and return loss (RL), (b) Isolation (ISO).

TABLE I. Simulated P1dB for Designed Switches

Frequency (GHz)	DPDT1	DPDT2
1	20.5	19.4
10	20.5	19.5
30	19.6	19.2

The simulated S-parameters of DPDT1 and DPDT2 are shown in Fig.3. Simulated insertion loss/isolation of DPDT1 (75/100/75) switch under 3.3 V bias are better than 1.6 dB/48 dB from DC to 30 GHz, and better than 1.8 dB/38 dB from 30 to 50 GHz, measured insertion loss/isolation of DPDT2 (150/100/150) switch under 3.3 V are better than 1.2 dB/37 dB from DC to 30 GHz. Simulated 1dB compression point (P_{1dB}) for DPDT1 and DPDT2 switches are around 19 to 20 dBm at different frequencies from 1 to 30 GHz, as shown in Table I

TABLE II COMPARISON OF WIDEBAND SWITCHES

	Tech.	Type	BW (GHz)	IL (dB)	ISO (dB)	Input P1dB (dBm)	Chip Size (mm^2)	Topology
[1]	GaAs JFET	2x2	DC-2	< 0.6	> 25	35	0.68 x 0.87	Ring-type
[2]	0.5 µm pHEMT	2x2	DC-6	1.1	> 25	34.5	na	Series only, ring-type
[3]	PIN diode	2x2	3.3-3.8	< 2	80	38.1	na	Shunt only, ring-type
[4]	0.13 µm CMOS	2x2	2-12	1.3 – 2.3	> 40	11-12	0.84x0.79	series-shunt-series, ring-type with matching networ
This work	**0.13µm SOI**	**2x2**	**DC-50**	**< 1.2 at 30 GHz < 1.8 at 50 GHz**	**> 37 > 28**	**>19**	**0.28 x 0.21**	**series-shunt-series, ring-type, with matching network, (> 3 kΩ–cm) substrate**

and a comparison of wideband switches is given in Table II against the proposed design's simulation results.

IV. CONCLUSION

DC-50 GHz DPDT switch matrixes have been introduced. The developed switches exhibit excellent performance at an ultra-wide frequency band from DC to across millimeter-wave.

ACKNOWLEDGMENTS

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