A Wideband Digital Variable Gain Amplifier with DC Offset Cancellation in SiGe 0.18μm BiCMOS Technology

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***Abstract*—This paper presents a five-stage wideband digital controlled variable gain amplifier (DVGA). A bandwidth extended technique is proposed in this design to enhance gain flatness and enlarge gain range in high operating frequency. DC offset cancellation in this design helps to enhance the performance of proposed DVGA. The design is simulated using a commercial 0.18μm SiGe BiCMOS technology. The DVGA has a simulated gain range of 64.7 dB with a 3-dB bandwidth from 3 MHz to 3.55 GHz, an output 1-dB gain compression point better than -5.2 dBm, an input return loss better than 11.9 dB, an output return loss better than 18 dB, and a dc power consumption for core DVGA circuit of 3.7 mW from a 1.8-V supply.**

***Index Terms*—Digitally controlled, low power design, millimeter wave, silicon germanium (SiGe) BiCMOS, 60-GHz communication, variable gain amplifier (VGA).**

I. Introduction

The high-speed wireless communications is becoming more and more important as portable devices get more powerful. As one of the most promising candidates for next generation communication, 60 GHz wireless system could achieve higher data rate due to the availability of at least 5 GHz bandwidth. Growing of silicon process technologies and low cost integration solutions have also make it possible to commercially realize transceivers working at these frequencies [1], [2].

As shown in Fig. 1, the digital variable gain amplifier (DVGA) is a fundamental building block in such wireless transceivers as signal received from antenna or digital base band modem usually has time-varying power [3], [4], [5]. VGA is usually set before the ADC to provide constant amplitude output voltages. According to IEEE 802.11ad standard, the bandwidth of communication channel is required to be approximately 2 GHz. DVGAs are therefore claimed to provide wide bandwidth and flat gain for different gain, together with low power consumption and high linearity [6], [7].

This paper proposes a low-power, high-linearity, more than 60-dB dynamic range DVGA for 60GHz wireless communication system. The DVGA consists five stages with DC offset cancellation (DCOC) functionality. A bandwidth extension technique is proposed to decrease the bandwidth variation within the gain range.

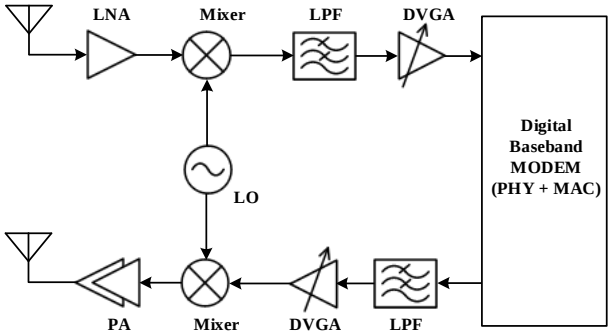


Fig. 1. DVGA application for transceiver.

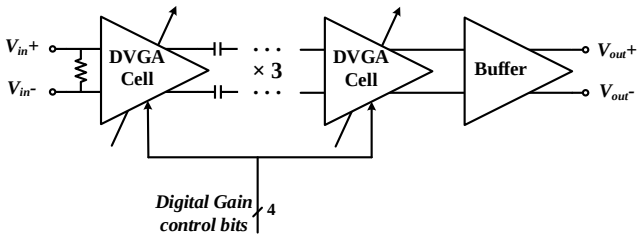


Fig. 2. Topology of the proposed DVGA.

II. DVGA Circuit Implementation

The proposed DVGA has five amplifier stages, which are shown in Fig 2. Each DVGA cell attributes a maximum gain of 8.5 dB. AC coupling circuits between amplifier stages provide a DCOC functionality to reduce noise figure in baseband and to prevent signal saturation of baseband signals. The proposed modified Cherry Hooper amplifier cell with bandwidth extension technique is shown in Fig 3. M_1 and M_2 are the main active devices of two cascaded differential common source amplifier. Resistors R_1 and R_2 are loads of M_2. M_3 and R_3 compose the feedback loop, which has been proved to enhance GBW of the circuit. Current biases of M_1 is designed to be digitally controllable to control the overall gain of DVGA circuit [8], [9], [10]. The transconductance of M_3, g_{m3}, is the dominant factor affecting the bandwidth of modified Cherry Hooper Amplifier when the controllable bias current is varied.

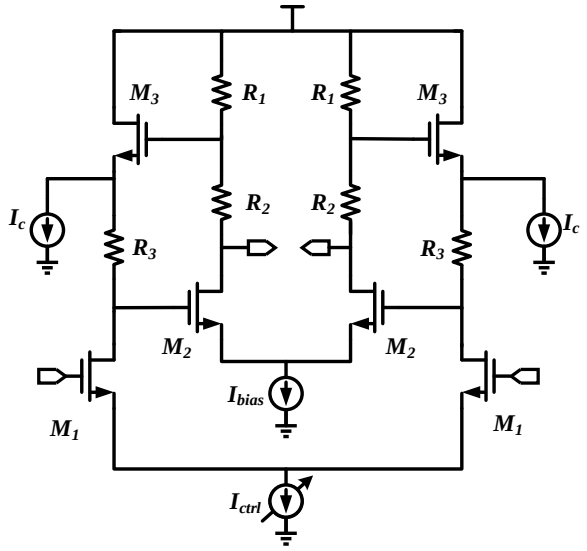


Fig. 3. Circuit schematic of the proposed DVGA cell.

The proposed compensated current I_c is introduced to the source of M_3 in order to enlarge bandwidth in lower gain setting region.

III. Simulation Results

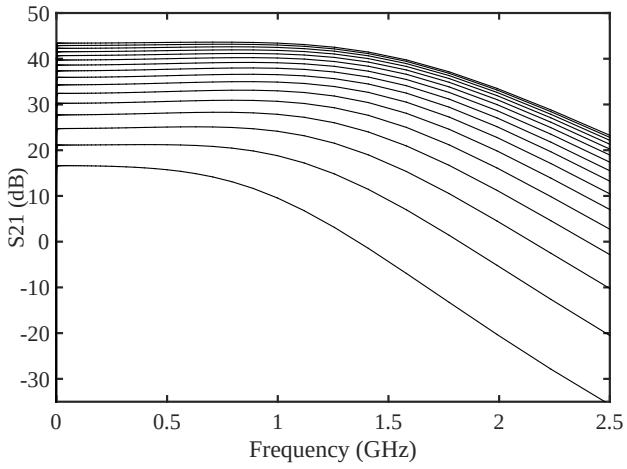
Fig. 4 shows the simulated comparison results for frequency response with and without the compensated current I_c. Fig. 4(a) indicates that bandwidth drops significantly to smaller than 1.5 GHz as the gain is set low if I_c is not compensated. On the other hand, the gain range is also limited in a smaller region due to the drop of g_{m3} in lower gain setting. As shown in Fig. 4(b), the compensated current helps to extend the bandwidth in the whole gain range, which also makes the variable gain region larger. A bandwith from 3 MHz to more than 3.55 GHz and a gain variation from -22.4 dB to 42.3 dB are achieved from the proposed DVGA.

Fig. 5 presents the simulated results of input and output return loss performance. The differential input is matched to 100 Ω by an input resistor. The output is matched by an output buffer which consumes a relative high power of 36 mW in order to avoid affecting the linearity of previous amplifier stages. As a result, the input return loss is better than 11.9 dB and output return loss is better than 18 dB for all gain setting.

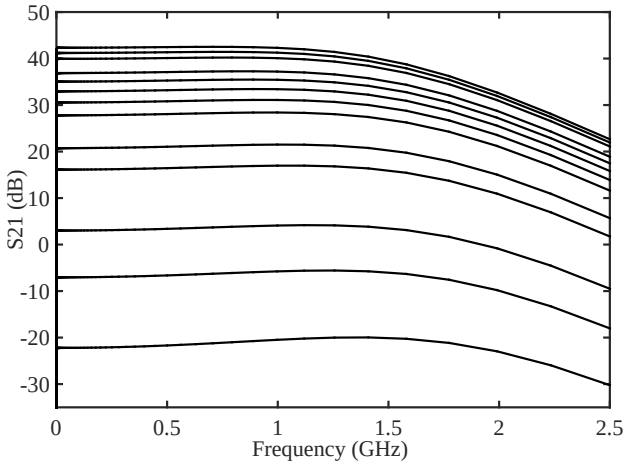
The overall performance of the proposed DVGA is compared with the state-of-the-art VGA designs and is compiled in Table I. The proposed DVGA design has the on-chip DCOC features. Linearity, bandwidth, gain range and power consumption are trade off between each other in DVGA design. The performance of this design is comparable with state-of-the-art designs.

IV. Conclusion

This paper proposes a DVGA topology and design techniques in 0.18μm SiGe BiCMOS technology. The VGA has



(a)



(b)

Fig. 4. Simulated frequency response of DVGA circuit (a) without bandwidth extended technique; (b) with bandwidth extended technique.

achieved simulated gain control of 64.7 dB with a bandwidth of 3 MHz to 3.55 GHz with DCOC functionality. The proposed bandwidth extended technique provides enhanced and robust performance that are essential for the wideband applications.

V. Acknowledgements

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TABLE I
PERFORMANCE SUMMARY OF STATE-OF-THE-ART VGA

Parameter	*This work	[11]	[12]	[13]	[14]
Technology	**0.18μm BiCMOS**	0.18μm BiCMOS	180nm CMOS	130nm CMOS	0.18μm BiCMOS
Gain range	**-22.4 to 42.3 dB**	-16.5 to 6.5 dB	1.6 to 40.2 dB	-5 to 66 dB	-1.4 to 30.2 dB
3-dB bandwidth	**3 M to 3.55 GHz**	DC to 5.6 GHz	DC to 148 MHz	20 MHz	3 M to 1.7 GHz
Power consumption	**3.7 mW**	7.9 mW	7.56 mW	1.1 mW	35 mW
Output P1dB	**-5.2 dBm**	-21.5 dBm	-3 dBm	NA	NA
Noise Figure	**26.1 dB**	16.5 to 27.1 dB	NA	NA	27 dB
On-chip DCOC	**Yes**	No	Yes	No	Yes

*Pre-layout simulation results

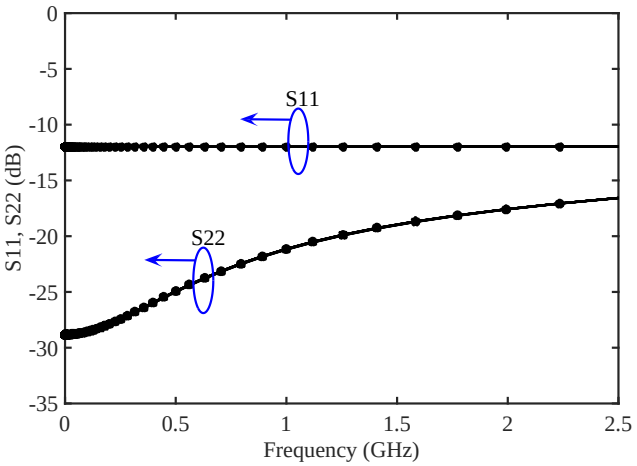

Fig. 5. Simulated input and output return loss for the proposed DVGA.

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