An Inductorless Transimpedance Amplifier Design for 10 Gb/s Optical Communication using 0.18-μm CMOS

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***Abstract*—This paper presents a novel inductorless transimpedance amplifier (TIA) design using Global Foundaries 0.18-μm CMOS technology suitable for high speed optical communication. A modified-RGC preamplifier stage (M-RGC) is used to lower input impedance through cascode and parallel PMOS transistor techniques for wideband operation. The amplifier stage used common source amplifiers to increase the gain and the third-order interleaving feedback technique to increase the bandwidth. The proposed TIA has a transimpedance gain of 59.5 dBΩ with bandwidth of 6.16 GHz and a power consumption of 21.2 mW (core power = 17.5 mW) for V_{DD} = 1.8 V.**

Keywords: Bandwidth enhancement, optical receiver, regulated cascode (RGC), transimpedance amplifier (TIA)

I. Introduction

Research in optical communications have increased in importance as the demand for greater data rates increased. The optical receiver front-end plays a critical role in determining the dynamic range, bandwidth and sensitivity for the whole network. The front end of the optical receiver includes the photodiode, TIA and Limiting Amplifier (LA) [1].

The dominant high-speed digital communication standard today is SONET OC-192 with 10 Gb/s being important [1]. This is because of several reasons. Firstly, the short-reach 10 Gb/s data communication standards have less stringent optical sensitivity requirements versus those of long-haul standards. Secondly, 10 Gb/s silicon photodetectors are compatible to the inexpensive 850 nm wavelength vertical cavity surface emitting lasers (VCSEL) extensively used for optical communications [2].

There are many tradeoffs between different desired parameters such as gain, bandwidth, noise, power consumption, chip area, sensitivity and dynamic range when designing for the TIA [3], among which gain, bandwidth and power consumption being the critical parameters most researchers focus on.

For TIA, the major bandwidth limiting factor is the capacitive load from the input photodiode due to its large area to capture sufficient light. This and additional capacitance from electrostatic discharge (ESD) protection and pads contribute to the dominant pole that limit the bandwidth of the TIA. Thus many TIA designs try to isolate or compensate the pole.

Although multi-order LC ladder networks or inter-stage inductive peaking can be used to increase bandwidth, this paper only considered inductorless techniques because on-chip spiral inductors require large amounts of area, power [2] and higher crosstalk resulting in performance degradation [4].

II. Traditional TIA Designs

TIA designs could be grouped into 2 categories which are shunt-shunt feedback TIA and regulated cascode TIA (RGC). The TIA can be single-ended or differential. An advantage of differential TIA is that the differential signal between the real and dummy photodetector is amplified and the common-mode signal is canceled, giving a high Common Mode Rejection Ratio (CMRR) to reject common-mode noise from the power supply or substrate coupling noise [5]. However this comes at a cost of chip area and power consumption as duplicate components are needed. Thus this paper would only consider single-ended TIA designs.

A. Shunt-shunt feedback TIA

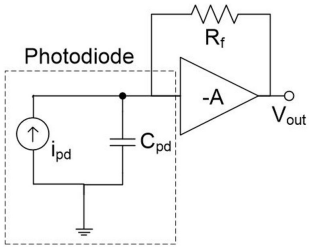

Fig. 1. Shunt-shunt feedback TIA

In this TIA design an amplifier with an open loop gain of A has a resistive feedback R_F across it in a feedback loop as shown in Fig. 1 [3]. In simulation, the photodiode is represented as an AC current source i_{pd} and a capacitor C_{pd}. If the open loop gain A is large enough and at low frequency,

the transimpedance is approximately -R_F [6]. Otherwise, the gain is calculated as [3]:

$$Z_T = \frac{V_{out}}{I_{in}} = \frac{-A}{A+1} * \frac{R_F}{1 + \frac{R_F C_{pd}}{A+1} s} \tag{1}$$

-3dB bandwidth is calculated as [3]:

$$f_{-3dB} \approx \frac{1}{2\pi} * \frac{A}{R_F C_{pd}} \tag{2}$$

The goal is to achieve Butterworth response whereby the frequency response graph is maximally flat [7]. There is a tradeoff regarding the size of R_F. If R_F is too small, it would result in worse gain (gain = R_F when A is large) and higher noise, reducing sensitivity. However if R_F is too large, it would result in lower bandwidth and close loop instability [6].

B. Regulated Cascode (RGC) TIA

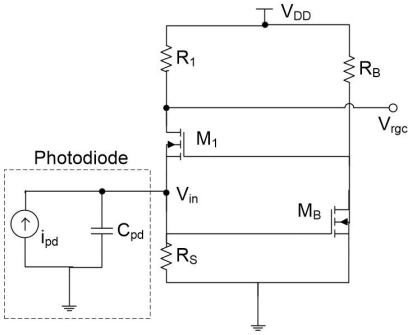

Fig. 2. Regulated Cascode (RGC) TIA

RGC design shown in Fig. 2 has been a popular design since its introduction due to its low input impedance and high output impedance [8]. To reduce the input impedance of the conventional CG (common-gate) input stage, the source input is also fed into the input of a CS (common-source) amplifier and the output fed back to the gate of the CG transistor. This results in the input impedance equal to $1/g_{m1}(1 + g_{mB}R_B)$ instead of $1/g_{m1}$ for CG alone, hence increasing the transconductance G_m by the factor $(1 + g_{mB}R_B)$. The lower input impedance of the RGC enables better isolation of the large photodiode capacitance from bandwidth determination [9].

Transimpedance gain is calculated as [8]:

$$Z_T = \frac{V_{out}}{I_{in}} \approx \frac{R_1}{[1 + s\frac{C_{pd}+C_i}{g_{m1}(1+g_{mB}R_B)}][1 + sR_1(C_L + C_o)]} \tag{3}$$

where $C_i \approx C_{sb1}$, $C_o \approx C_{gd1} + C_{db1}$ and C_L is the capacitive load of subsequent stages.

The low frequency transimpedance gain $Z_T(0)$, its input impedance $Z_{in}(0)$ and -3dB bandwidth are calculated as [8][10]:

$$Z_T(0) = \frac{V_{out}}{I_{in}} \approx R_1 \tag{4}$$

$$Z_{in}(0) \approx \frac{1}{g_{m1}(1 + g_{mB}R_B)} \tag{5}$$

$$f_{-3dB} \approx \frac{1}{1 + sR_1(1 + \frac{g_{m1}}{g_{mB}}C_{gd1} + (C_{db1} + C_L))} \tag{6}$$

where C_L is the capacitive load.

Thus there are 2 poles which can be calculated:

$$f_{p2} = \frac{1}{2\pi * \frac{C_{pd}+C_i}{g_{m1}(1+g_{mB}R_B)}} \tag{7}$$

$$f_{p1} = \frac{1}{2\pi * R_1(C_L + C_{gd1} + C_{db1})} \tag{8}$$

The pole in (7) is determined at the input node V_{in} and the pole in (8) is determined at the output node V_{rgc}. The pole in (7) is the dominant pole due to the very small input resistance [8]. This makes the bandwidth still dependent on the photodiode capacitance.

III. Proposed TIA Preamplifier Stage Design

For our design, RGC TIA was chosen over shunt-shunt feedback TIA. This is because the gain-bandwidth tradeoff is highly dependent on R_F for shunt-shunt feedback TIA. However, for RGC TIA both the gain and bandwidth rely on slightly different parameters shown in (4) and (6) respectively and thus can be further tuned for optimization.

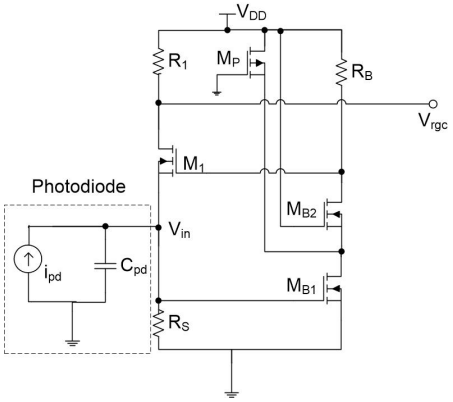

Fig. 3. Proposed modified RGC Preamplifier Stage

Despite the RGC stage lowering the input impedance, it cannot totally isolate the large input parasitic capacitance on the bandwidth. Thus 2 additional bandwidth enhancing techniques are required. The proposed TIA preamplifier stage is a modified RGC stage with cascode transistor M_{B2} and parallel PMOS M_P techniques as shown in Fig. 3.

A. Cascode transistor M_{B2}

Although the RGC has a lower input impedance than CG, the existence of C_{gd1} and the Miller effect of M_B in RGC also causes bandwidth limitation as shown in (6). A cascode transistor M_{B2} is added at the source of the CS M_{B1} and the gate of the CG M_1 and has a gate voltage of V_{DD} [10].

Additionally, signal analysis reveals that the input impedance is not affected by the additional cascode, thus not affecting the bandwidth for input impedance [10].

B. Parallel PMOS M_P to R_B and M_{B2}

By adding a parallel PMOS M_P, the CS amplifier is formed by M_P and M_{B2} which provides an even larger transconductance $g_{mMB2}(g_{mMB1} + g_{mMP})$ for the feedback transistor M_{B1} and thus lowers the input impedance and isolates the pole in (7) even more, increasing the bandwidth [11].

The input impedance of our preamplifier stage:

$$Z_{in}(0) \approx \frac{1}{g_{m1}(1 + g_{mB2}(g_{mB1} + g_{mP}))} \tag{9}$$

The BW of our modified RGC, similar to [10]:

$$f_{-3dB} \approx \frac{1}{1 + sR_1(C_{gd1} + (C_{db1} + C_L))} \tag{10}$$

Thus by using the using cascode M_{B2} and the parallel PMOS M_P, the dominant pole is now pole (8) at V_{rgc} because the input pole (8) at V_{in} have become totally isolated.

IV. TIA Amplifier Stage Design

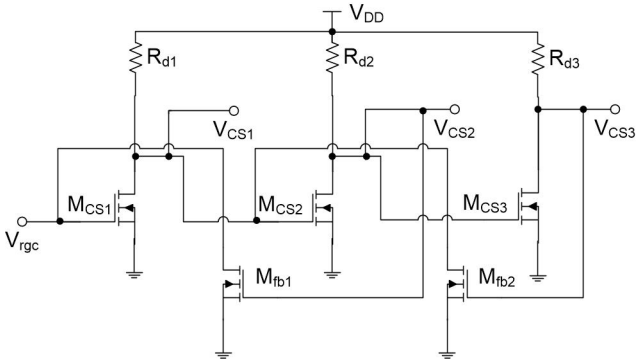

Fig. 4. Proposed 3-order Interleaving Amplifier Stage

The amplifier stage is necessary in order to increase the gain from the RGC output since the signal is still too small for subsequent stages. Our amplifier stage shown in Fig. 4 is a third-order interleaving feedback which is a method to ensure that the amplifier stage does not decrease the bandwidth from the preamplifier stage. It consists of a cascaded feedforward 3-stage CS amplifiers with 2 CS feedbacks in between [12]. An advantage of using active over passive feedback components is that there is less process variation during manufacturing [13].

Assuming each node has a load of $R_L//(1/sC_L)$, the transfer function is given as [12]:

$$\frac{V_{CS3}}{V_{rgc}}(s) = -\frac{A^3(s)}{1 + 2A^2(s)A_f(s)} \tag{11}$$

where $A(s) = A/\frac{A}{1+s/2\pi f_0}$ and $A_f(s) = A_f/\frac{A_f}{1+s/2\pi f_0}$ are the feedforward and feedback paths respectively and $f_0 = 1/(2\pi R_L C_L)$, R_L = resistive load of each stage and C_L = capacitive load of each stage. All 3 feedforward stages are taken to be identical and both feedback stages are taken to be identical for simple calculation.

There are 3 poles obtained in the transfer function [12]:

$$f_{p1} = -f_0(1 + \sqrt[3]{2A^2A_f}) \tag{12}$$

$$f_{p2,3} = -f_0(1 - \frac{1}{2}\sqrt[3]{2A^2A_f} \pm j\frac{\sqrt{3}}{2}\sqrt[3]{2A^2A_f}) \tag{13}$$

The 2 active feedback loops Af1 and Af2 pushes the pole to a higher frequency as shown in (12) [12]. The high frequency peaking of both Af1 and Af2 which can be now be used to extend the bandwidth is calculated as [13]:

$$f_{Af1,peak} = \frac{1}{2\pi * R_{d1}(C_{gdCS2} + C_{gdAf1})} \tag{14}$$

$$f_{Af2,peak} = \frac{1}{2\pi * R_1(C_{gdCS1} + C_{gdAf2})} \tag{15}$$

The buffer stage is a simple source follower with resistive load that acts as a voltage buffer to match to 50 Ω.

V. Results and Discussion

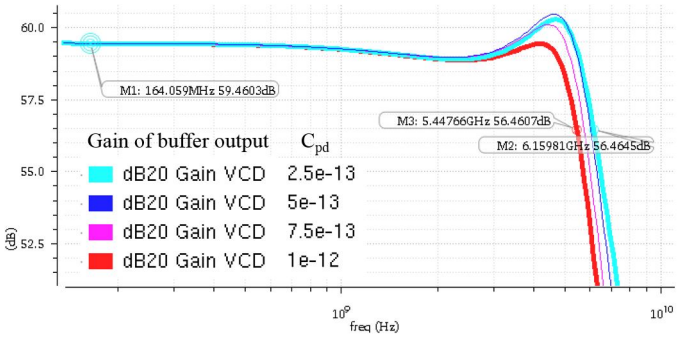

Fig. 5. Frequency Analysis in Cadence Schematic while varying C_{pd}

Fig. 5 shows the frequency response of the proposed TIA circuit. The gain can be determined as 59.46 dBΩ and bandwidth as 6.16 GHz for C_{pd} = 0.25 pF. Power consumption is 21.18 mW (core circuit = 17.5 mW). When C_{pd} is increased to 1 pF (300% increase), gain remains constant and bandwidth decreases to 5.44 GHz (16% decrease), hence demonstrating great resilience to input capacitance variation.

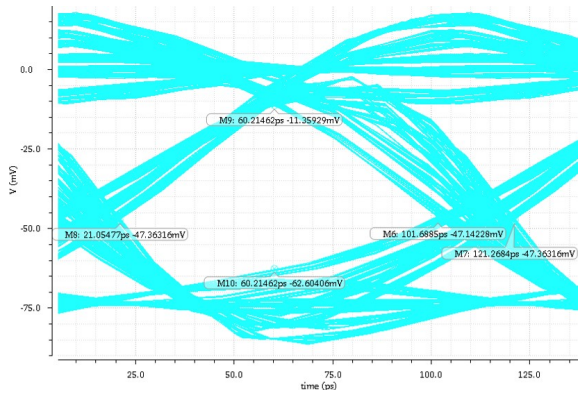

Fig. 6. Eye diagram for 10 Gb/s PRBS signal

Fig. 6 shows the eye diagram of the proposed TIA circuit for the 10 Gb/s Pseudo Random Binary Sequence (PRBS) signal. The eye is clear and open with a horizontal opening of 80 ps and a vertical opening of 51 mV. This proves that the design works for both periodic and aperiodic signals. The peak to peak jitter = 20 ps.

A standard figure of merit (FOM) calculated as (16) is used to compare with other recent inductorless TIA designs in Table 1 below.

$$FOM = \frac{Gain(\Omega) * Bandwidth(GHz) * C_{pd}(pF)}{DC\,power(mW)} \quad (16)$$

Table 1: Comparison of this work with previous works

Reference	[14]	[15]	[16]	[17]	**This Work**
Technology (nm)	90	28	90	180	**180**
Input capacitance (pF)	0.3	0.19	0.15	0.05	**0.25**
Gain (dBΩ)	63.5	56	59	54.3	**59.46**
Gain (Ω)	1496	630	891	518	**940.3**
Bandwidth (GHz)	6	10	9.6	7	**6.16**
DC power without buffer (mW)	12	18	N/A	N/A	**17.5**
DC power with buffer (mW)	60	56	45	29	**21.18**
FOM with buffer (Ω*(GHz)*pF/mW)	44.8	21.4	28.5	6.2	**68.4**

There are several advantages of our design. Firstly, as shown in Table 1, our work provides reasonable gain and bandwidth for the lowest power consumption, especially for the buffer stage. Secondly, due to the isolation of the input capacitance C_{pd}, our design allows a large variation of C_{pd} without much bandwidth loss. Thirdly, our design has no physically large components such as inductors or capacitors that results in a large chip size.

VI. Conclusion

In conclusion, a new inductorless RGC TIA design is shown in GlobalFoundaries 0.18-μm CMOS technology, which gives a good FOM tradeoff between gain, bandwidth and power consumption for 10 Gb/s optical communication, is less affected by input capacitance and is expected to take up a very small amount of chip space.

VII. Acknowledgment

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