

An Inductorless Variable-Gain Transimpedance Amplifier Design for 4GHz Optical Communication using 0.18- μm CMOS

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Abstract. *This paper presents a novel variable-gain inductorless transimpedance amplifier (TIA) design using Global Foundries 0.18- μm CMOS technology which is suitable for high speed optical communication. A modified-RGC (M-RGC) preamplifier stage is used to reduce the input impedance through cascode and parallel PMOS transistor techniques for wideband operation. The amplifier stage uses common source amplifiers to increase the gain and an interleaving feedback technique to increase the bandwidth. The amplifier stage also has variable open-loop and resistive close-loop control mechanisms to vary the gain depending on the input signal strength without causing instability or a decrease in bandwidth. The proposed TIA has a transimpedance gain range of 45.4 dB Ω to 62.2 dB Ω for a dynamic range from 0.2 μA_{pp} to 600 μA_{pp} . It has a bandwidth above 4.3 GHz throughout this range and a core dc power consumption of 7.72 mW (total dc power with buffer is 9.48 mW) for 1.8 V supply voltage.*

Introduction

Due to the demand for faster data transmission speeds for optical communication, it is increasingly important to research on improving the different circuit blocks in the transmitter and receiver systems. The first circuit block in the receiver is the transimpedance amplifier (TIA), which determines many parameters such as the bandwidth, sensitivity and dynamic range of the entire receiver system [1] and thus is the most critical block in the system.

SONET OC-192 [1] is an important high-speed standard for digital communication. This is because it allows low-cost 850 nm wavelength vertical cavity surface emitting lasers (VCSEL) to be used to emit signals [2]. There are two pressing issues in TIA designs today. Firstly, a critical tradeoff occurs between the gain and bandwidth. Most researchers try to increase the transimpedance limit curve outwards with a high gain and high bandwidth in their designs [3]. The main cause of a limited bandwidth is due to the capacitive load from the photodiode, electrostatic discharge (ESD) protection and pads (grouped together as C_{pd}) at the TIA input which lowers the dominant pole frequency and reduces the bandwidth. Thus this paper has come up with an effective way to isolate the input capacitance from affecting the bandwidth.

Secondly, there is a limited dynamic range for the input signal. Dynamic range refers to the ratio between the maximum to minimum input photocurrent suitable for the optical receiver [4]. A large dynamic range is desired because there is a large variation in received optical signal power [5] and to prevent saturation [4]. The lower limit is

fixed by the sensitivity of the TIA, which is determined by the noise, while the upper limit is determined by the distortion and nonlinearity of the large input signal usually because of the voltage headroom issue [4]. This paper solves the issue of the upper limit by devising an innovative variable gain design that is adaptive to the input signal strength. Thus when the input signal increases beyond a limit, the gain would proportionally decrease while maintaining the bandwidth.

This paper has considered inductorless design techniques because on-chip spiral inductors require a larger area [2] and results in higher crosstalk that degrades performance [6].

Regulated Cascode (RGC) TIA

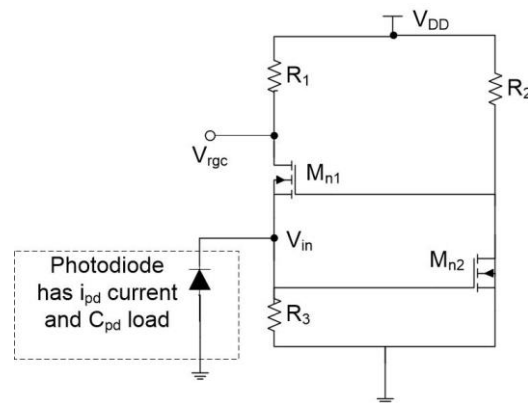


Figure 1. Standard Regulated Cascode (RGC) TIA

The RGC design shown in Figure 1 is common because of its low input impedance as compared to a conventional CG (common-gate) input stage [7]. The photodiode current signal goes into both the input of a CG and a CS (common-source) amplifier, with the CS output fed back to the gate of the CG transistor. This results in the input impedance lowered to $1/g_{mn1}(1 + g_{mn2}R_2)$ instead of $1/g_{mn1}$ for the CG itself. A lower input impedance of the RGC allows better isolation of the input capacitive load [6].

Transimpedance gain is calculated as [7]:

$$Z_T = \frac{V_{out}}{I_{in}} \approx \frac{R_1}{(1+s\omega_1)(1+s\omega_2)} \quad (1)$$

$$\omega_1 = \frac{C_{pd}}{g_{mn1}(1 + g_{mn2}R_2)} \quad (2)$$

$$\omega_2 = R_1(C_o + C_{amp}) \quad (3)$$

Where $C_o \approx (1 + g_{mn1}/g_{mn2})C_{gdn1} + C_{dbn1}$ and C_{amp} is capacitive load of the subsequent amplifier stage

The zero frequency transimpedance gain $Z_T(0)$ and its input impedance $Z_{in}(0)$ are calculated as [7]:

$$Z_T(0) \approx R_1 \quad (4)$$

$$Z_{in}(0) \approx \frac{1}{g_{mn1}(1 + g_{mn2}R_2)} \quad (5)$$

For the 2 poles that are calculated, the pole in (2) is determined at the input node V_{in} and the pole in (3) is determined at the output node V_{rgc} . Although the input impedance

is reduced, the input pole (2) is still the dominant pole due to the large capacitive load C_{pd} .

Automatic Gain Control (AGC)

An AGC circuit has an active and inactive mode. During the inactive mode, there is no change in the gain and bandwidth as input signal increases. However, in the active mode, the AGC circuit lowers the gain in an automatic and proportional manner. Hence this increases the dynamic range by raising the input signal upper limit [4]. This allows larger input signals into the TIA without being distorted by the voltage headroom issue at the last gain stage with the largest amplification.

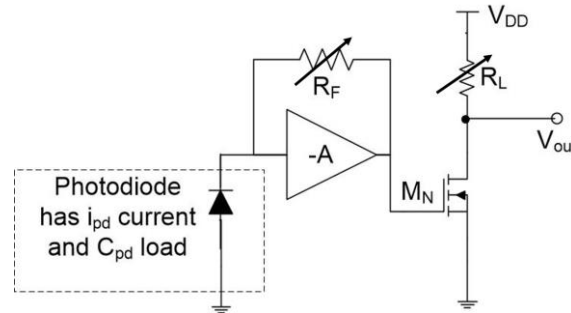


Figure 2. Example of the close-loop variable R_F and open-loop variable R_L

As shown in Figure 2, the 2 main methods of varying gain are to vary the close-loop resistor R_F or to vary the open-loop resistor R_L [5]. The variable resistors are created by transistors biased in the linear region with varying input gate voltages [9].

Varying the Close-loop Resistor R_F

R_F refers to the feedback resistor across a negative gain stage and is a direct contributor of the gain of a shunt-shunt feedback TIA. If sufficiently large, the gain at zero frequency is equivalent to R_F [10]. When R_F is reduced, the amount of feedback current is increased and thus increases gain loss of the open-loop amplifier.

In an AGC circuit, as the input signal increases till the upper limit, R_F should be slowly reduced in order to reduce the gain. Hence R_F is implemented using a PMOS/NMOS transistor that has a varying V_{gs} that decreases/increases respectively.

Varying the Open-loop Resistor R_L

R_L refers to the load resistor of a common-source amplifier stage that contributes to the gain of that stage. The ideal gain of a common-source stage is taken to be $-g_m R_L$. Thus reducing the resistance directly reduces the gain of the stage. Both variable R_F and R_L are used in the design as they have complementary advantages explained later.

Proposed TIA Preamplifier Stage Design

The proposed RGC TIA preamplifier design is the same as that previously presented in [11].

The RGC stage has 2 additional bandwidth-enhancing techniques that increase the isolation of C_{pd} from bandwidth determination, the first being a cascode transistor M_{n3} and second being a parallel PMOS M_{p1} to R_2 and M_{n3} as shown in Figure 3.

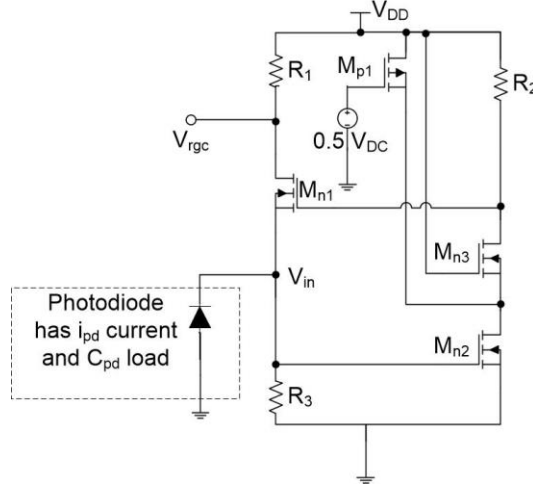


Figure 3. Proposed modified RGC Pre-amplifier Stage

Parallel PMOS M_{p1} to R_2 and M_{n3}

With an additional parallel PMOS M_{p1} , the CS amplifier formed by M_{p1} and M_{n2} provides a greater transconductance $g_{mn3} || (g_{mn2} + g_{mp1})$ for the feedback transistor M_{n2} , hence lowering the input impedance and isolating C_{pd} . The dominant pole shifts from pole (2) to (3), hence increasing the bandwidth [12].

The input impedance of the pre-amplifier stage:

$$Z_{in}(0) \approx \frac{1}{g_{mn1} \{1 + [g_{mn3} || (g_{mn2} + g_{mp1})] R_2\}} \quad (6)$$

The bandwidth after addition of parallel PMOS:

$$f_{-3dB} \approx \frac{1}{2\pi} \times \frac{1}{R_1 \left(\left(1 + \frac{g_{mn1}}{g_{mn2} + g_{mp1}}\right) C_{gdn1} + C_{dbn1} + C_{amp} \right)} \quad (7)$$

Where C_{amp} is the input capacitive load of the subsequent amplifier stage transistors

$$C_{amp} = C_{gdCS1} + C_{gsCS1} + C_{gdRF1}$$

Cascode Transistor M_{n3}

C_{gdn1} and M_{n2} Miller effect in RGC also restricts the bandwidth as shown in (7). A cascode transistor M_{n3} is added between the drain of the CS M_{n2} and the gate of the CG M_{n1} and with a gate voltage of 0.5 V. This aids in overcoming the Miller effect $(1 + g_{mn1}/(g_{mn2} + g_{mp1}))C_{gdn1}$ and lowers the influence of C_{gdn1} on the bandwidth of the dominant pole [13].

Combined Gain and BW of Proposed TIA Pre-amplifier

Gain and bandwidth of Pre-amplifier Stage at V_{rgc} from I_{in} :

$$Z_{pre} = \frac{R_1}{(1+s\omega_{pre1})(1+s\omega_{pre2})} \quad (8)$$

$$\omega_{pre1} = \frac{C_{pd}}{g_{mn1} \{1 + [g_{mn3} || (g_{mn2} + g_{mp1})] R_2\}} \quad (9)$$

$$\omega_{pre2} = R_1 (C_{gdn1} + C_{dbn1} + C_{amp}) \quad (10)$$

$$f_{-3dB} \approx \frac{1}{2\pi} \times \frac{1}{R_1(C_{gdn1} + C_{dbn1} + C_{amp})} \quad (11)$$

Although the bandwidth equation is similar to [13], this proposed design has better isolation due to M_{p1} that ensures that the dominant pole of the design follows (11) more closely than [13].

Proposed TIA Amplifier Stage Design

The proposed TIA amplifier design consists of 3 CS stages with an active interleaving feedback and an additional AGC function over that previously designed by the authors in [11].

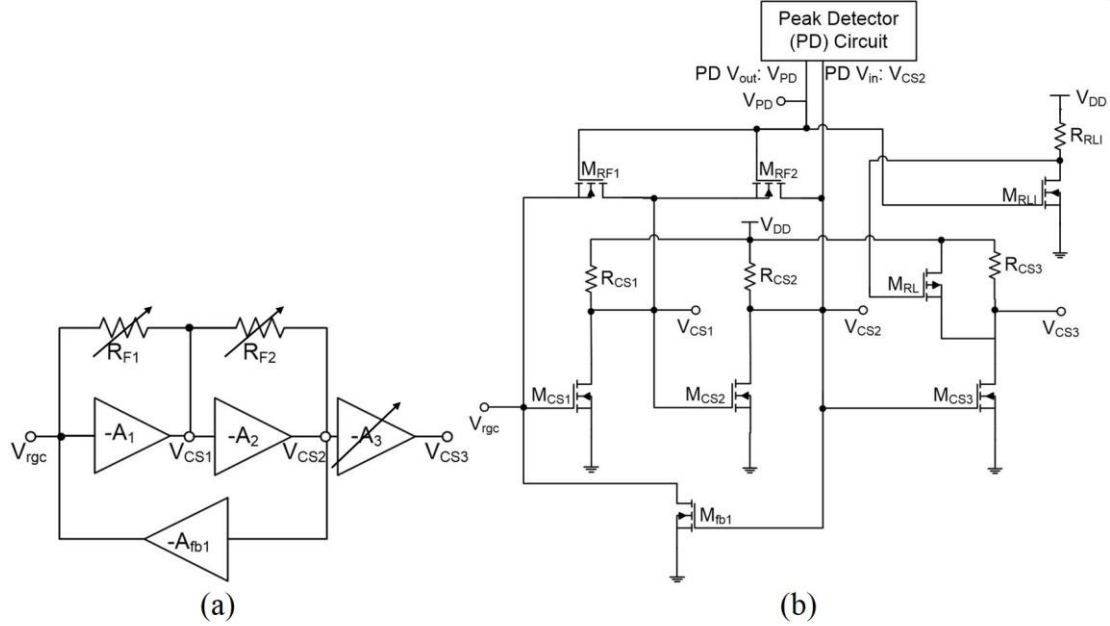


Figure 4. (a) Simplified and (b) transistor-level Proposed Amplifier Stage

The amplifier stage is necessary in order to increase the gain from the RGC output since the signal is still too small for subsequent stages. The amplifier stage shown in Figure 4. There are 2 main innovative techniques in the amplifier stage. Firstly, an interleaving feedback transistor M_{fb1} helps to increase the bandwidth. Secondly, there is an adaptive gain circuit using variable feedback resistors M_{F1} , M_{F2} and M_L .

There are several factors that contribute to poles in the amplifier stage. Firstly, each CS has a pole contributed by the load resistor and capacitance of the subsequent stage. Secondly, M_{fb1} contributes to the pole of the combined first and second stages. Thirdly, M_{F1} , M_{F2} and M_L contributes to the poles of the first, second and third stages respectively. We calculated the contributed poles of the 2 innovation techniques separately and then combined them together.

Active Interleaving Feedback Transistor M_{fb1}

The 1 CS feedback in between [14] which is M_{fb1} creates an active feedback loop A_{fb1} . An advantage of using active over passive feedback components is that there is less process variation during manufacturing [15]. Calculating the contribution of A_{fb1} alone first, it generates a high frequency peaking caused by the introduction of a zero that helps increase the bandwidth and can be calculated as in [15]:

$$f_{A_{fb1}, peak} = \frac{1}{2\pi} \times \frac{1}{R_{o,rgc}C_{o,rgc}} \quad (12)$$

Gain at V_{CS2} from V_{rgc} when accounting for only M_{fb1} could be estimated similar to [14]:

$$\frac{V_{CS2}}{V_{rgc}} = \frac{\left(\frac{A_1}{1+s\omega_{amp1}}\right)\left(\frac{A_2}{1+s\omega_{amp2}}\right)}{1 - \left(\frac{A_1}{1+s\omega_{amp1}}\right)\left(\frac{A_2}{1+s\omega_{amp2}}\right)\left(\frac{A_{fb1}}{1+s\omega_{fb1}}\right)} = \frac{A_1 A_2 (1+s\omega_{fb1})}{(1+s\omega_{amp1})(1+s\omega_{amp2})(1+s\omega_{fb1}) - A_1 A_2 A_{fb1}} \quad (13)$$

$$\omega_{amp1} = \frac{1}{R_{d1}C_{o,CS1}} \quad (14)$$

$$\omega_{amp2} = \frac{1}{R_{d2}C_{o,CS2}} \quad (15)$$

$$\omega_{fb1} = \frac{1}{R_{o,rgc}C_{o,rgc}} \quad (16)$$

Where $A_1 = g_{mCS1}R_{CS1}$, $A_2 = g_{mCS2}R_{CS2}$ and $A_{fb1} = g_{mfb1}R_{o,rgc}$ with $R_{o,rgc}$ being the output resistance of the previous RGC stage into the first amplifier stage CS and where $C_{o,CS1} = (C_{gdCS1} + C_{gsCS2} + C_{gsRF1} + C_{gdRF2})$, $C_{o,CS2} = (C_{gdCS2} + C_{gsCS3} + C_{gdfb1} + C_{gsfb1} + C_{gsRF2} + C_{gdfb1} + C_{gsfb1})$ and $C_{o,rgc} = (C_{gdRF1} + C_{gdCS1} + C_{gsCS1} + C_{gdfb1})$ which are defined as the load capacitances to V_{CS1} , V_{CS2} and V_{rgc} respectively.

AGC Variable Transistors R_{F1} , R_{F2} and R_L

A good AGC design would incorporate both varying R_F and R_L that would complement each other. A previous implementation in [5] controls both digitally. However, because it is a 6-bit binary control, it requires 6 parallel PMOS transistors in an array for varying both R_F and R_L , which increases chip area. In addition, this also requires an additional analog-to-digital converter (ADC) circuit.

The AGC circuit which is fully analog controlled contains 3 variable resistors R_{F1} , R_{F2} and R_L that are controlled by the same input voltage V_{PD} from a peak detector circuit, which provides an increasing dc voltage from 1.2 V to 1.75 V as the small-signal current input from the photodiode increases from 0.2 μA_{pp} to 600 μA_{pp} , which is within the input current range from photodiodes [5].

R_{F1} and R_{F2} are closed-loop NMOS variable resistors across the first CS and second CS stages respectively, while R_L is an open-loop PMOS variable load resistor of the third CS stage. NMOS resistors are used for R_{F1} and R_{F2} because of the output voltage of the peak detector that bias the gate, while an additional CS stage consisting of M_{RL1} and R_{RL1} flips the input signal to bias the PMOS R_L , which is preferred over NMOS due to the constant biasing source voltage of V_{DD} .

The gain and bandwidth of each node in the amplifier stage (V_{CS1} , V_{CS2} and V_{CS3}) can be calculated with the simplification of the active feedback loop A_{fb1} not taken into consideration.

Gain at V_{CS1} from V_{rgc} :

$$\frac{V_{CS1}}{V_{rgc}} = \frac{-A_1}{1 - A_1} \times \frac{1}{1 + s\omega_{amp3}} \quad (17)$$

$$\omega_{amp3} \approx \frac{(R_{CS1} || R_{F1} || R_{F2})C_{o,CS1}}{1 - A_1} \quad (18)$$

Where $R_{F1} = r_{dsRF1}$ of M_{RF1} and $R_{CS1} || R_{F1} || R_{F2}$ because they are all connected to V_{CS1} and taken to have approximately the same voltage dc voltage across for easy calculation.

Gain at V_{CS2} from V_{CS1} :

$$\frac{V_{CS2}}{V_{CS1}} = \frac{-A_2}{1 - A_2} \times \frac{1}{1 + s\omega_{amp4}} \quad (19)$$

$$\omega_{amp4} \approx \frac{(R_{CS2} || R_{F2}) C_{o,CS2}}{1 - A_2} \quad (20)$$

Where $R_{F2} = r_{dsRF2}$ of M_{RF2} and $R_{CS2} || R_{F2}$ because both are connected to V_{CS2} and taken to have approximately the same voltage dc voltage across for easy calculation.

Although gain shown in (17) and (19) decreases as R_{F1} and R_{F2} decreases respectively, the bandwidth decreases instead of increasing due to the increase in parasitic C_{gd} and C_{gs} of these transistors which contribute to $C_{o,CS}$. Thus a compensation technique is used by adding the variable R_L as well. Since R_L is parallel to R_{CS3} , the gain of that stage is equivalent to $-g_{mCS3}(R_{CS3} || r_{dsRL})$.

Gain at V_{CS3} from V_{CS2} :

$$\frac{V_{CS3}}{V_{CS2}} = -A_3 \quad (21)$$

Where $A_3 = g_{mCS3}(R_L || R_{CS3})$, $R_L = r_{dsRL}$ of M_{RL} .

As shown in (21), when R_L decreases the gain also decreases. The bandwidth will increase, which compensates for the decrease in bandwidth caused by the decrease in R_{F1} and R_{F2} . This creates a nearly constant bandwidth no matter the variable gain of the AGC and ensures that it works properly.

Gain at V_{CS3} from V_{rgc} when accounting for only M_{F1} , M_{F2} and M_L :

$$\frac{V_{CS3}}{V_{rgc}} = - \frac{A_1 A_2 A_3}{(1 - A_1)(1 - A_2)(1 + s\omega_{amp3})(1 + s\omega_{amp4})} \quad (22)$$

Combined Gain of Proposed TIA Amplifier

For calculated gains in (13) and (22), care needs to be taken to prevent duplication when calculating M_{fb1} and M_{F1} , M_{F2} and M_L separately.

The combined gain of V_{CS3} from V_{rgc} :

$$Z_{amp} = \frac{A_1 A_2 A_3 (1 + s\omega_{fb1})}{\{(1 + s\omega_{amp1})(1 + s\omega_{amp2})(1 + s\omega_{fb1}) - A_1 A_2 A_{fb1}\} \{(1 - A_1)(1 - A_2)(1 + s\omega_{amp3})(1 + s\omega_{amp4})\}} \quad (23)$$

Where C_{buffer} is the load capacitance of the next stage which is the buffer. The bandwidth of the Amplifier stage is taken to be the bandwidth of the third CS stage as it is the limiting stage.

Combined Gain of Entire Proposed TIA

Gain at V_{CS3} from I_{in} :

$$Z_{TIA} = Z_{pre} \times Z_{amp} \quad (24)$$

The buffer stage after the gain stage is a source follower with resistive load that acts as a voltage buffer to match to 50 Ω .

Results and Discussion

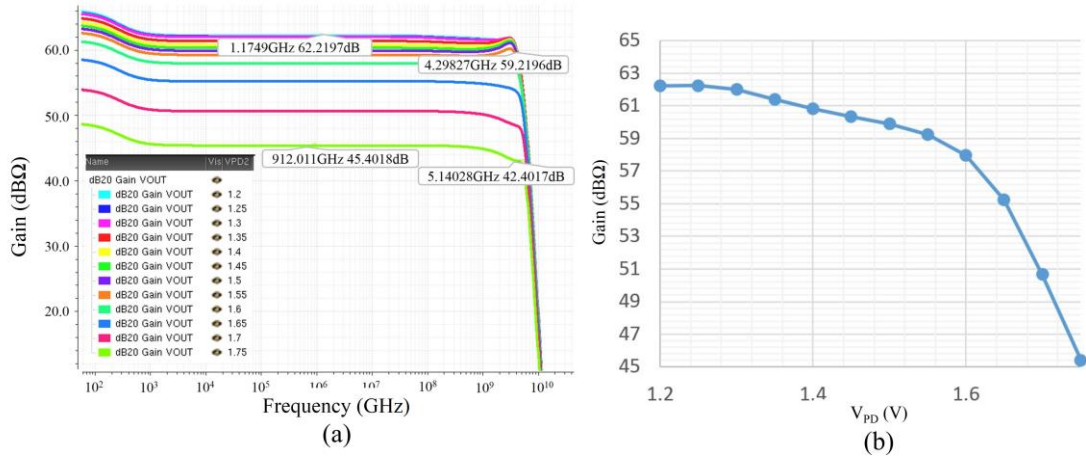


Figure 5. (a) Frequency response with varying V_{PD} and (b) Gain variation versus V_{PD}

Figure 5(a) shows the frequency response of the proposed TIA circuit. The maximum gain during the inactive mode of the AGC is measured at 62.22 dBΩ and bandwidth is maintained above 4.3 GHz for $C_{pd} = 0.25$ pF as V_{PD} increases with increasing input photodiode current. The usable frequency range is from 1 kHz to a constant 3dB bandwidth of above 4.3 GHz.

Figure 5(b) shows the Gain versus V_{PD} graph from the results in 5(a). As can be seen, from 1.2 V till 1.3 V, the AGC is inactive and the gain decreases minimally. Above 1.3 V, in the active mode, the AGC increasingly lowers the gain to a minimum of 45.4 dBΩ when it reaches 1.75 V. The maximum peaking of the graph occurs at $V_{PD} = 1.5$ V with a peak of 1 dBΩ. This shows that design is able to perform reliably as a variable gain AGC TIA.

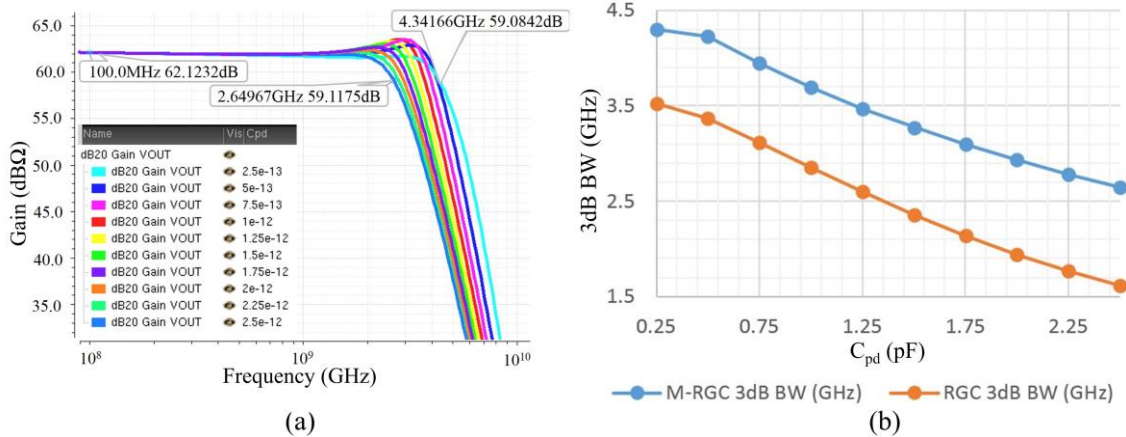


Figure 6. (a) Frequency Response with varying C_{pd} and (b) BW variation versus C_{pd}

In Figure 6(a), when C_{pd} is increased from 0.25pF to 2.5pF (1000%), the gain remains constant and bandwidth decreases from 4.3 GHz to 2.65 GHz (drop 38.4%). The maximum peak of 1 dBΩ occurs at $C_{pd} = 0.75$ pF. In Figure 6(b) not only is the bandwidth at $C_{pd} = 0.25$ pF higher (by 0.78 GHz), it also drops more slowly compared to the standard RGC input stage (with identical component parameters) with a gain of 61.35 dBΩ (0.87 dBΩ difference). Hence this demonstrates great resilience to input capacitance variation and input capacitance isolation of the bandwidth enhancing techniques.

A standard figure of merit (FOM) calculated as (25) is used to compare with other recent AGC TIA designs in Table 1 below.

$$FOM = \frac{Gain (\Omega) \times Bandwidth (GHz) \times C_{pd} (pF) \times Gain Range (max dB\Omega - min dB\Omega)}{DC Power of core circuit (mW)} \quad (25)$$

	[16]	[5]	[17]	This Work
RF CMOS Technology (nm)	180	180	180	180
Input Capacitance (pF)	0.25	0.9	0.25	0.25
Maximum Gain (dBΩ)	53.8	66	69.3	62.22
Maximum Gain (Ω)	490	1995	2917	1291
Minimum Gain (dBΩ)	44.6	48	55.8	45.40
Minimum Gain (Ω)	170	251	616	186.2
Gain Range (max dBΩ - min dBΩ)	9.19	18	13.5	16.82
Bandwidth (GHz)	9.1	1.5	1	4.3
Core dc power (mW)	30	27	6	7.72
FOM	341	1795	1641	3021

Table 1. Comparison of this work with previous works

As shown in Table 1 above, the proposed design has a better FOM compared with other recent papers. Firstly, the gain range of 16.82 dBΩ which is the second highest proves that the proposed variable R_{F1} , R_{F2} and R_L design is effective. Secondly, bandwidth of 4.3 GHz is also the second highest which proves the proposed bandwidth enhancing techniques in the RGC input stage and AGC amplifier stage. Thirdly, the core dc power of 7.72 mW is also the second lowest.

There are several advantages of the proposed design. Firstly, as shown in Table 1, the proposed design provides reasonable gain and bandwidth for a low power consumption. Secondly, due to the isolation of the input capacitance C_{pd} , the design allows a large variation of C_{pd} without much bandwidth loss. Thirdly, the design utilizes an innovative gain variation technique while maintaining bandwidth. Lastly, the design is fully analog controlled without any analog-to-digital converter (ADC) and digital control components for the AGC. It also has no inductors. Thus these factors help to ensure a small chip size.

Conclusion

This paper shows an inductorless variable-gain RGC TIA design using Global Foundries 0.18-μm CMOS technology. Not only does it have new bandwidth enhancing techniques that protects the large input capacitive load from bandwidth determination, it also has a novel method of varying the gain by maintaining a high bandwidth.

Acknowledgements

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