A 4 GHz 60 dB Variable Gain Amplifier With Tunable DC Offset Cancellation in 65 nm CMOS

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***Abstract*—This letter presents a compact CMOS based variable gain amplifier with 60 dB gain control range and a feedback reconfigurable dc offset cancellation. The design is a four-stage fully differential cascaded amplifier implemented using a 65 nm CMOS process. The amplifier achieves a current controllable gain range from -39.4 dB to $+20.2$ dB, a voltage tunable lower cutoff frequency from dc to 200 kHz, a consistent 3 dB bandwidth better than 4 GHz, a maximum dc power consumption of 26 mW, a measured in-band group delay variation of 20 ps, and a noise figure from 10 to 27 dB. The proposed VGA design occupies a compact die area of only 75 μm $\times$ 80 μm (excluding pads for measurement).**

***Index Terms*—CMOS VGA, DC offset cancellation, low power design, tunable DCOC, variable gain amplifier (VGA).**

I. Introduction

VARIABLE gain amplifiers (VGA) are used in RF transceivers to control the good link budget for reliable wireless communication. The VGA provides an interface between RF transceiver and the baseband chipset by regulating the signal power level within the baseband input dynamic range. However, the dc component in the baseband spectrum along with the manufacturing mismatch related offset voltage amplification may saturate the following stages in the baseband circuitry and introduce non-linearity effects [1]. To prevent this non-linear effect, a CMOS high gain VGA that can provide a dc rejection by using the dc offset cancellation (DCOC) either by forward path high pass filtering (HPF) or by feedback low pass filtering (LPF) is required [1]. By providing a higher DCOC cutoff frequency as a band pass filter (BPF) response, a good dc offset suppression can be achieved to meet the BER requirement of the specified baseband standard [2].

For the receiver chain, a high signal to noise ratio (SNR) at the baseband is also a critical specification for the majority of the baseband communication standards [1]. Some of the energy in the baseband spectrum is crowded at dc [2] and SNR at the receiver baseband input gets degraded due to a higher DCOC corner frequency [6]. However, a lower cutoff frequency close to dc results in a marginal DCOC along with a long settling time due to any spontaneous change of the VGA gain [2]. To overcome these two complementary circuit requirements from the baseband standards, many reconfigurable RF frontend to broadband interface techniques are proposed in the literature such as switching between VGAs with and without DCOC [3], by using active RC filter with switched capacitors [4], by using dual-mode channel-select filters by switching between complex high order LPF and BPF implemented by an operational amplifier based auto-tuned RC filters [5], by using lumped capacitor and resistor arrays that are switched for tuning [6] and by using current mode programmable complex integrator [7]. However, these works have limitations such as the redundancy of the duplicated circuitry leading to large die area, added circuit complexity involving high order filters, additional power consumption by using active filters and additional losses with delays in the RF signal path that are introduced by the parasitic components.

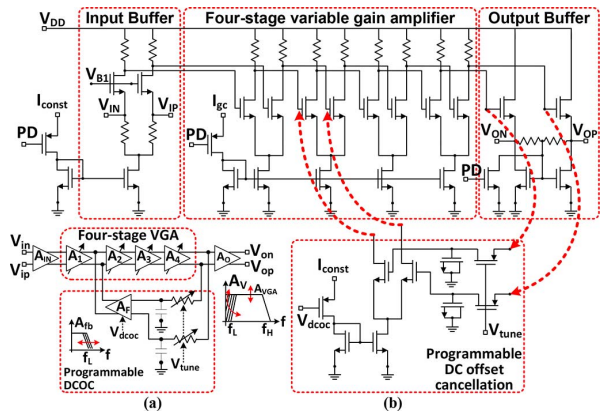

Fig. 1. (a) Block diagram and (b) circuit schematic of the proposed VGA.

In this letter, the proposed VGA circuit provides a flexibility of turning ON/OFF the DCOC functionality by using a digital switch along with a voltage controlled lower cutoff frequency that can provide a compromise between the baseband SNR and BER requirements. Hence by providing this reconfigurable capability in the VGA design, the RF transceivers can support multi-standard baseband [1] interface by switching between the direct conversion receiver (DCR), i.e., zero-IF (direct conversion scheme) and the tunable low-IF (superheterodyne) receiver schemes [5].

II. Circuit Topology and Design

The proposed design is a compact variable gain amplifier shown in Fig. 1 with four sub-blocks namely input buffer, four-stage VGA core, output buffer and programmable DCOC. To ensure low power consumption, the design is biased using NMOS current sinks mirrored from the stable current sources ($I_{\rm const}$ and $I_{\rm gc}$). The input stage is a common gate amplifier to provide fixed gain biased by using $I_{\rm const}$ current ($\approx$ 50 μA) and wideband input impedance matching independent of the

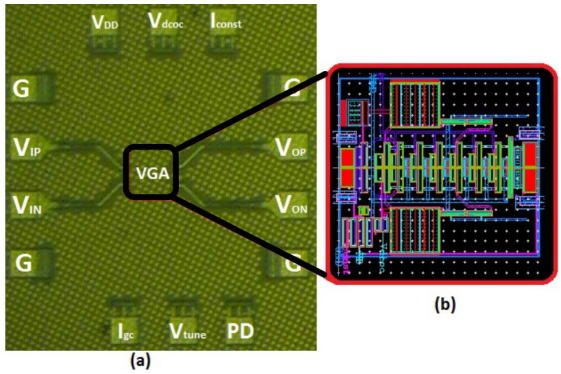

Fig. 2. (a) Die microphotograph (b) Layout of the proposed CMOS VGA.

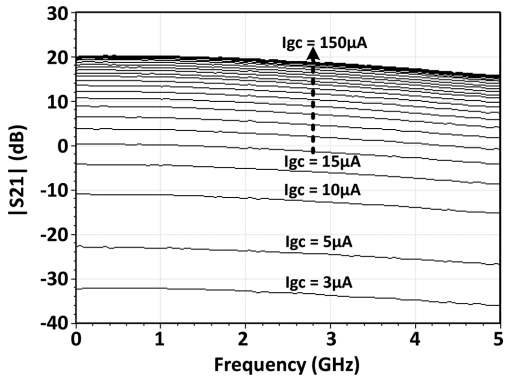

Fig. 3. Measured VGA gain (I_{gc} = 3 to 150 μA, step = 5 μA).

VGA gain. The VGA core comprises of four-stage common source amplifier with resistive load to provide wideband gain flatness. The output buffer is a source follower with common mode feedback circuit providing a stable output common mode voltage and a good output impedance matching. The programmable DCOC comprises of a MOS transistor based RC LPF that extracts the dc from output and cancels it with the input of the second stage by using a differential amplifier as shown in Fig. 1(b).

When $V_{\rm dcoc} = 1.2$ V, the DCOC functionality is turned OFF by using a PMOS switch, thus the VGA forward path has a low pass filter response apparently allowing the dc component to pass to the baseband section and conversely when $V_{\rm dcoc} = 0$ V, the DCOC functionality is activated, thus extracting the dc component from the output and cancelling the dc signal from the RF input signal. The VGA lower cutoff frequency is tunable by using $V_{\rm tune}$ control voltage which varies the channel resistance of the PMOS pass transistor in the DCOC LPF. This DCOC functionality with variable lower cutoff frequency provides a flexibility to configure the receiver RF frontend interface based on the baseband standard specification with better tradeoff between the baseband processing efficiency with improved SNR against the circuit dc offset effects, i.e., the BER specification.

The size of the lumped RC components used in a DCOC LPF depends on the VGA operating frequency and it is usually very large for frequencies close to the baseband. To avoid large die area and high fabrication cost, the RC components of the LPF are implemented by using the MOS transistors. The large resistor value is implemented by using PMOS transistors operated in the triode region with the gate voltage controlling the channel resistance and is given by

$$R_{ch} \cong \left[\mu_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_P \cdot (V_{\rm DD} - V_{\rm tune} - |V_{\rm THP}|)\right]^{-1} \quad (1)$$

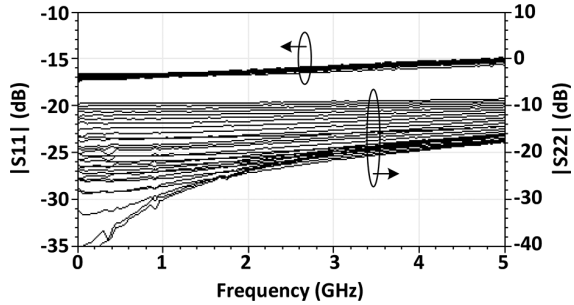

Fig. 4. Measured VGA return loss ($I_{\rm gc}$ = 3μA to 150 μA, step = 5μA).

where $\mu_p, C_{ox}, ((W)/(L))_P$ and $V_{\rm THP}$ are the electron mobility, gate oxide capacitance per unit area, aspect ratio, and threshold voltage of the LPF PMOS transistors.

The fixed large shunt capacitor is designed by using NMOS transistor with the source and drain connected to GND as the bottom plate and the gate terminal as the top capacitor plate. This makes the design very compact and easily integrated for mobile applications.

III. Experimental Results

The proposed design is fabricated by using Global Foundries 65 nm CMOS technology. The die microphotograph of the proposed VGA along with the layout is shown in Fig. 2. The VGA occupies a compact die area of 75 μm $\times$ 80 μm (excluding measurement pads) and 510 μm $\times$ 620 μm (with measurement pads for the testability). The measured data is obtained by on-wafer probing with the Agilent E8364B network analyzer and HP 8970B noise figure meter by using differential calibration. The measured variable gain and the input/output return loss are shown in Figs. 3 and 4, respectively, by varying $I_{\rm gc}$ from 3 to 150 μA. The tunable DCOC is achieved by activating the digital switch ($V_{\rm dcoc} = 0$ V) and by controlling the VGA's lower cutoff frequency by varying $V_{\rm tune}$ from 0 to 1.2 V as shown in Fig. 5. From Fig. 5(a) with minimum gain setting ($I_{\rm gc} = 3\ \mu$ A) a passband gain drop is seen when the DCOC lower cutoff frequency is increased by decreasing $V_{\rm tune}$ from 1.2 V to 0 V which is not observed in Fig. 5(b) for maximum VGA gain ($I_{\rm gc} = 150\ \mu$A). This behavior is caused by the subtraction of the lower forward path signal (VGA minimum gain) with the increasing feedback signal due to reduced DCOC LPF loss (series R_{ch} of the PMOS pass transistor is decreasing) that increases the VGA passband attenuation. Although this does not affect the baseband interface performance, since for the VGA minimum gain, the dc component along with the input RF signal is also attenuated preventing saturation of the baseband circuitry due to dc offsets and additionally it enhances the VGA gain control range. The monotonous trend of the measured gain and the noise figure against $I_{\rm gc}$ is shown in Fig. 6. The linearity performance based on $\rm P_{1dB}$ plots for a maximum ($I_{\rm gc} = 150\ \mu$A), mid ($I_{\rm gc} = 30\ \mu$A) and minimum ($I_{\rm gc} = 5\ \mu$A) VGA gain is consolidated in Fig. 7. The maximum measured in-band group delay variation over the entire VGA gain range is 20 ps.

The measured results of the proposed VGA are summarized and compared with the state-of-the-art VGAs [8]–[13] in Table I. The proposed CMOS VGA has better bandwidth, compact die area and tunable DCOC while achieving comparable gain range and dc power consumption as compared to the CMOS based VGAs [8]–[11]. The dc power consumption of [11] is lower than the proposed design. However, for the

TABLE I
MEASURED PERFORMANCE SUMMARY OF THE STATE-OF-THE-ART VGA

Parameters	Units	This Work	[8]	[9]	[10]	[11]	[12]	[13]
Technology	-	**65nm CMOS**	90nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	0.18μm SiGe HBT	0.18μm SiGe HBT
Gain range	dB	**-39.4 to +20.2**	-29 to +23	+3 to +31	-25.3 to +59	-10 to +50	-16.5 to +6.5	-1.4 to +30.2
3-dB bandwidth	Hz	**(0~0.2 M) to 4 G**	0.8 G	20 M to 0.98 G	1 G	0.1 M to 2.2 G	5.6 G	3 M to 1.7 G
Noise Figure	dB	**10 to 27**	-	6 to 21	15.2 to 50	17 to 30	16.5 to 27.1	23.5 to 52
Input P_{1dB}	dBm	**-17 to -30**	-15 to -26	-4 to -31	~+9 to -70.1	-13 to -55	-17 to -27	-9 to -36
Core Area	μm^2	**75 × 80**	71 × 490	330 × 470	660 × 106	270 × 50	170 × 60	810 × 310
Power consumption	mW	**26**	31.2	48	21.9	2.5	7.9	35.3
On-chip DCOC	-	**Yes**	No	Yes	Yes	Yes	No	Yes
Tunable DCOC	-	**Yes (0 to 0.2 MHz)**	No	No	No	No	No	No
Gain control mode	-	**Analog current**	Digital voltage	Digital voltage	Digital voltage	Analog voltage	Digital current	Digital current

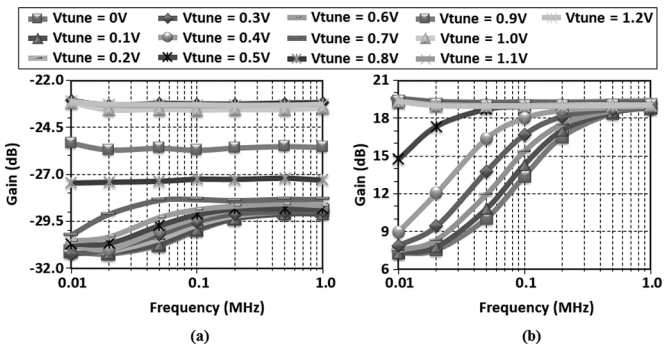

Fig. 5. Measured VGA low frequency response with and without the DCOC ($V_{dcoc} = 0$ V and $V_{tune} = 0$ to 1.2 V, step $= 0.1$ V) (a) $I_{gc} = 3\ \mu A$ (b) $I_{gc} = 150\ \mu A$.

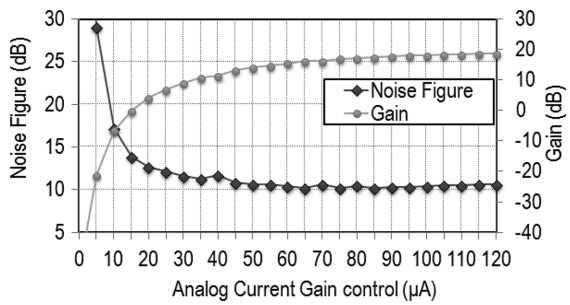

Fig. 6. Measured gain and NF at 1 GHz for $I_{gc} = 0$ to 120 μA, step $= 5\mu A$.

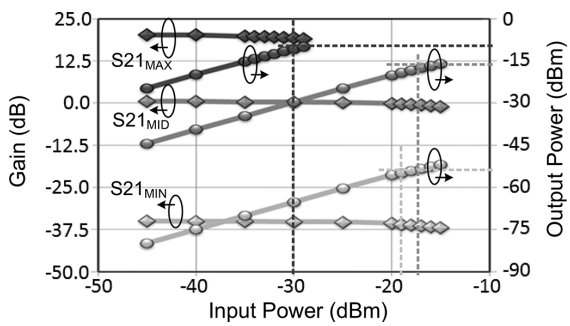

Fig. 7. Measured $P_{1\,dB}$ plot for maximum ($I_{gc} = 150\ \mu A$), mid ($I_{gc} = 30\ \mu A$) and minimum ($I_{gc} = 5\ \mu A$) VGA gain at 1 GHz.

purpose of measurement additional output buffer is necessary in [11]. As compared to the state-of-the-art SiGe HBT based VGA designs in [12], [13], the proposed VGA has improved gain range, tunable DCOC and compact die area. The power consumption and bandwidth of [12] is better than the proposed VGA design. However, the design in [12] lacks on-chip DCOC capability. The VGA design in [13] has passive RC based DCOC that occupies large die area.

IV. CONCLUSION

A compact variable gain amplifier with programmable DCOC capability is proposed and developed by using a commercial CMOS technology. The gain control range of 60 dB, compact size of 75 μm × 80 μm and wide operating bandwidth of over 4 GHz are achieved simultaneously. The programmable DCOC capability provides a better reconfigurable baseband interface to meet both the SNR and BER conflicting requirements of the baseband standards.

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