

A 26.8 dB Gain 19.7 dBm CMOS Power Amplifier Using 4-way Hybrid Coupling Combiner

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Abstract—This letter presents a novel compact 4-way hybrid coupling combiner applied in an mm-wave CMOS power amplifier (PA) design with wideband, large output power and high gain. Basing on the principle of both series and parallel combination concurrently working in a concentric distributed active transformer, the size of a 4-way power combiner can be dramatically reduced. Using the proposed power combiner, a four-stage common source PA is implemented in 65 nm CMOS process. In each stage, inductive source degeneration is employed to enhance transistor stability without reducing maximum stable gain. The measurement results show that the PA can offer 26.8 dB linear gain with 3 dB bandwidth of 51–67 GHz. At 1.2 V/1.4 V external supply voltage, the PA is able to deliver 17.5 dBm/19.7 dBm P_{sat} with 10.3%/13.4% power added efficiency (PAE). The chip size of the PA is only 0.32 mm².

Index Terms—4-way power combiner, hybrid coupling, power amplifier (PA), source degeneration, V-band.

I. INTRODUCTION

CMOS has become an attractive process for microwave and millimeter wave power amplifier (PA) design because of its feasibility of integration with other RF and baseband circuits toward system on chip (SOC). To overcome the limited power delivered by single MOSFET, several on-chip power combining techniques have been developed for high output power of PA [1]–[8]. Wilkinson [3], [6] and 2-D distributed [8] are on the basis of in-phase signal combination. As number of ways increases, more chip area for PA would be demanded. In distributed active transformer (DAT) PA [1], [2], [5], [7], transmission lines or inductors for power combining and impedance matching are generally folded to reduce size. Among DAT combiners, the type of dual-way in series can achieve good efficiency and phase balance for power combination [2]. For 4-way DATs, the power combination is mostly satisfied by duplicating dual-way combiners physically, as shown in Fig. 1(a). Accordingly, the combiner size is estimated to be doubled without considering interconnects [1], [5], [7].

In this work, to further reduce the size of 4-way DAT, a novel 4-way hybrid coupling combiner is proposed and illustrated in

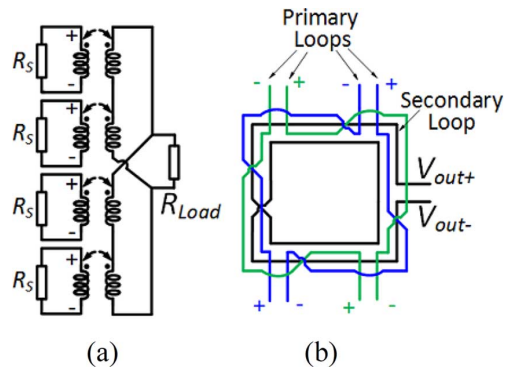


Fig. 1. 4-way combiner configurations. (a) 4-way combiner by paralleling dual way ones; (b) Proposed 4-way hybrid coupling combiner.

Fig. 1(b). In the proposed configuration, input power from either blue or green primary loops is combined in traditional series manner, while the parallel combining is formed by arranging another two primary loops with concentric winding. This method can dramatically reduce the size of a 4-way combiner as compact as a conventional dual-way combiner. The proposed 4-way DAT is used in a differential V-band PA design. Moreover, in each stage of the designed four-stage PA, inductive source degeneration (ISD) is used to increase stability while maintains maximum stable gain (MSG) of CMOS transistors.

II. 4-WAY HYBRID COUPLING COMBINER BASED PA DESIGN

A. PA Topology and ISD

The topology of this four-stage V-band CMOS PA is shown in Fig. 2(a). Each stage is consisted of DATs and pseudo-differential unit amplifiers (UAs). In the first stage, the differential input is further divided by a parallel DAT. Then 1:1 DATs are implemented for inter-stage matching from the output of UA1 to the input of UA3. Next, four UA4 blocks are driven by two UA3 blocks with the aid of series power splitters. Finally, the proposed 4-way hybrid coupling DAT is used for combining high output power. When UAs with 65 nm CMOS transistor are properly matched by these DATs, this four-stage PA can provide high gain at V-band. To compensate the gain roll-off effect of transistors and achieve wideband response, the DATs are optimized stage by stage for matching at higher frequency range with compromising of a little mismatching at lower frequency range.

In each UA, common source (CS) CMOS transistor pair with ISD is used for better stability. It is investigated that without ISD stabilization, oscillation risk of CMOS transistor increases as its total gate width increases because of more capacitance between gate and drain. In this work, the ISD is implemented

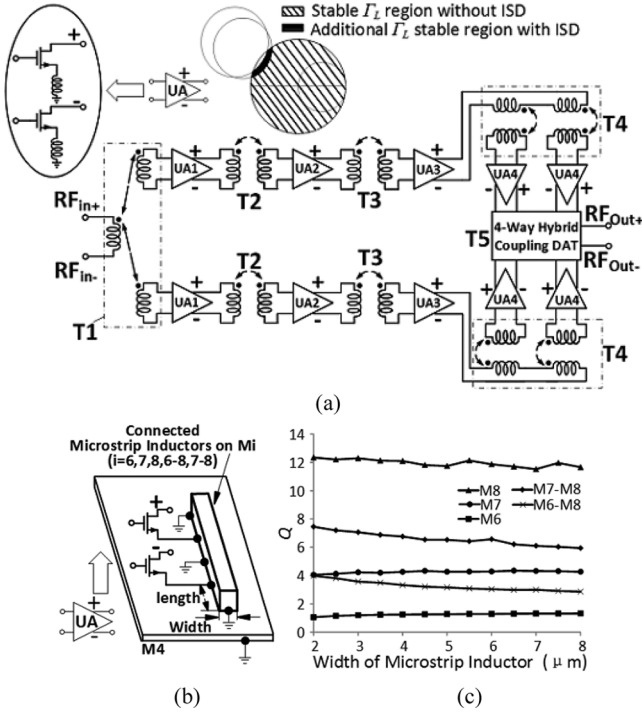


Fig. 2. (a) The proposed architecture of V-band DAT-based CMOS PA with ISD; (b) ISD connection diagram for a UA; (c) Simulated Q values of microstrip inductor with different layer options and trace width.

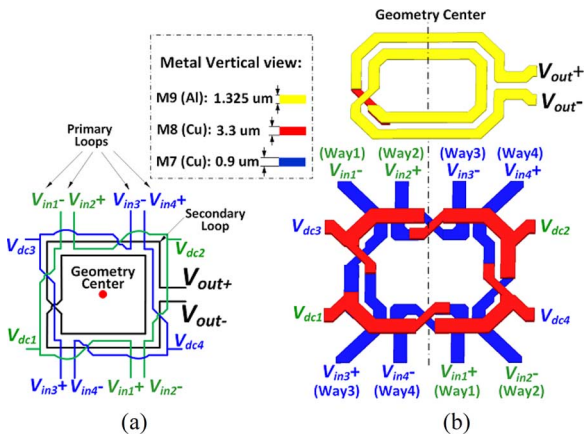


Fig. 3. (a) Winding topology of hybrid combiner T5, (b) Physical configuration of 4-way hybrid coupling combiner T5.

by connecting transistor source to the center of a microstrip inductor with two grounded terminals as illustrated in Fig. 2(b). Comparing the quality factors (Q) of the microstrip inductor under different layer options given in Fig. 2(c), the metal layer for making ISD is preferred to be M8 as denoted in Fig. 3. The inductor trace width is selected to be 3.5 μm for high Q and compact size. The total inductance of ISD is determined by the length of microstrip inductor. Through small signal simulation with transistors, the ISD inductance is designed within the range, in which MSG is not degraded. Table I shows the design parameters of UAs with and without ISD. It indicates that the stable region in Γ_L plane is enlarged by using ISD. The stable region for load selection of UAs with or without ISD is illustrated in Fig. 2(a).

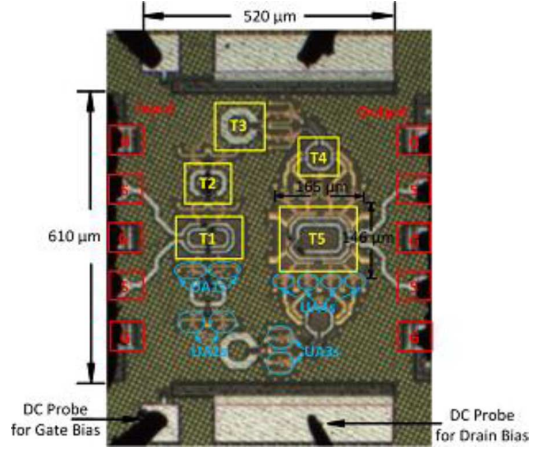


Fig. 4. Chip photograph of the fabricated 51–67 GHz CMOS power amplifier.

TABLE I
SIMULATED UA PARAMETERS W/ AND W/O ISD AT 60 GHz

Stage	Device Size (um)	Without ISD		With ISD		
		MSG (dB)	μ	Inductance (pH)	MSG (dB)	μ
UA1	50 \times 2	10.2	0.82	4.3	10.4	0.92
UA2	75 \times 2	10.2	0.74	4.5	10.5	0.86
UA3	100 \times 2	10.1	0.72	6.6	10.4	0.90
UA4	100 \times 2	10.1	0.72	4.1	10.4	0.84

μ : Edwards's stability parameter.

B. Four Way Hybrid Coupling DAT

To reduce the size of 4-way hybrid coupling DAT T5, the primary loops of two series transformers are placed around the same geometry center. The topology and physical structure are shown in Fig. 3(a) and (b) respectively. If only way 1 and way 2 (or way 3 and way 4) are taken into account, their voltage would be summed up by secondary loop in series manner. The coupling trace of each input way only occupies about one fourth length of concentric octagonal spirals. The parallel power combination is formed because the inner and outer winding sections from two input ways would double the output current in the secondary loop. The center tap of each primary loop is used for dc bias to UA4. For the 4-way hybrid coupling DAT, the impedance ratio T of one input referred to the output is mainly determined by physical winding ratio of their inductors. According to Load-Pull simulation of the transistor, the optimal load impedance for UA4 is $26.3 + j25.1 \Omega$. When the secondary loop has turn number of two, this scheme would theoretically transfer the input impedance seen by each UA4 to one fourth output load impedance of 100 Ω . Correspondingly, the ac current ratio of primary over secondary is around 2:1. To reduce overall power dissipation and improve efficiency, primary loops are designed on M7 and M8 with better conductivity. At 51–67 GHz, the insertion loss of each way from input to output is less than 2.0 dB. The phase and amplitude balance characteristics are investigated by full-wave EM simulation. When differential input is referred to way 1, the phase imbalance and amplitude imbalance are better than 12.4 degrees and 0.46 dB respectively.

III. EXPERIMENTAL RESULTS

The proposed PA is designed and fabricated in GF's standard 65nm CMOS process. The chip photograph is shown in Fig. 4.

TABLE II
SUMMARY OF THE STATE-OF-ART V-BAND CMOS PAs

Ref.	Tech. (nm)	Freq. (GHz)	Supply (V)	Gain (dB)	BW (GHz)	P_{-1} (dBm)	P_{sat} (dBm)	Area (mm ²)	PAE	$P_{sat}/Area$ (mW/mm ²)	GBWP (dB·GHz)	Combiner Area Per Way (mm ²)
[2]ISSCC2011	ST 65nm	60	1.0	20.3	12*	15.0	18.6	0.28	15.1	258.73	243.6	0.025
[3]ISSCC2010	ST 90nm	60.5	1.2	14.3	15	11.0	16.6	0.461	4.9	98.94	214.5	0.057
[5]ISSCC2010	IBM 65nm	60	1.0	19.2	10	15.4	17.7	0.83	11.1	70.94	192.2	0.075
[6]TMTT2013	TSMC 65nm	64	1.2	16.3	25.1	19.4	23.2	1.88*	10.0	111.13	409.3	0.023
[7]TMTT2013	ST 65nm	61	1.2	20	5*	13.5	15.6	1.15*	6.6	31.57	100.0	0.029
[8]TMTT2013	UMC 65nm	60	1.2	8.3	16	9.7	11	0.28*	7.1	44.96	132.8	0.017
[4]TMTT2013	TSMC 65nm	60	1.2	15.7	5.8	14.7	18.5	0.385	10.2	183.88	91.06	0.030
This Work	GF 65nm	60	1.2	26.6	16.0	14.3	17.5	0.32	10.3	175.73	425.6	0.006
This Work	GF 65nm	60	1.4	28.0	13.9	16.0	19.7	0.32	13.4	291.39	389.2	0.006

*: Estimated value from paper cited. BW is abbreviation of 3-dB bandwidth estimated by S-parameters.

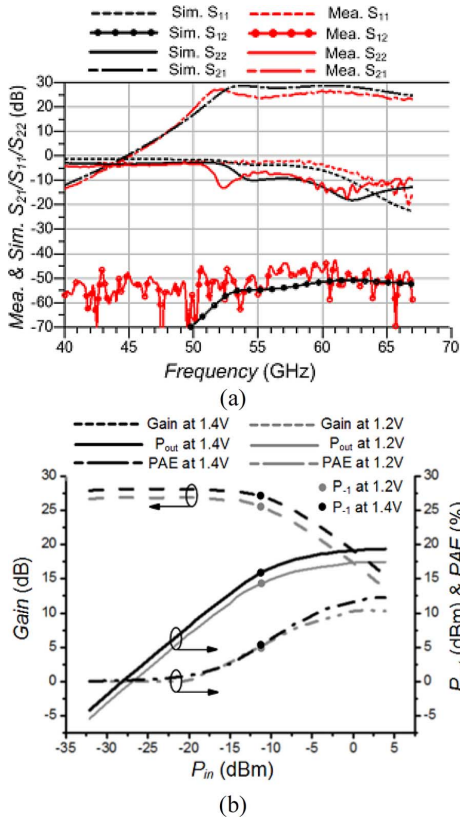


Fig. 5. (a) Measured and simulated S-parameters. (b) Measured Power gain, P_{-1} , P_{out} and PAE vs P_{in} at 60 GHz.

The core area of PA occupies $520 \times 610 \mu\text{m}^2$ and the size of T5 is $165 \times 146 \mu\text{m}^2$. Under small signal measurement, the S-parameters agree well with that of the simulation as illustrated in Fig. 5(a). The PA can provide more than 23.8 dB linear gain with 3 dB bandwidth of 16 GHz, i.e., 51 GHz – 67 GHz. The input return loss of the designed PA can be further improved through optimizing the transformer T1 and interconnects. The measured S_{12} is less than -43.5 dB for all tested frequencies. In Fig. 5(b), the large-signal test results show that the output 1 dB compression point (P_{-1}) is 14.3 dBm and the P_{sat} is 17.5 dBm with 10.3% PAE at 60 GHz when dc probe for drain is biased with 1.2 V. Since only two thin metal layers are used for connections between UAs and dc probes for drain bias, the voltage level at transistor drain of UAs would be lower than 1.2 V. In order to compensate bias degradation caused by parasitic series resistor, the probe voltage for drain bias is then set

to 1.4 V. The test results show that the output P_{-1} is increased to 16.0 dBm at 60 GHz while the P_{sat} is 19.7 dBm with 13.4% PAE . In Table II, the performance of this PA is compared with that of the state-of-arts. The designed PA achieves high gain and output power with compact area. For the power combiner part, it is of the smallest size and the chip area of each way occupies less than one fourth as compared to that of other configurations.

IV. CONCLUSION

In this letter, an mm-wave CMOS PA design with wideband, large output power and high gain is implemented in a commercial CMOS process. In each UA of the four-stage PA, ISD is employed to stabilize transistors and maintain their MSG . Benefiting from concentric winding topology of 4-way hybrid power combiner, the four-stage PA achieves compact size and high output power. The designed PA offers more than 23.8 dB linear gain from 51 to 67 GHz and demonstrates 19.7 dBm saturated output power with peak PAE of 13.4%. Although these aforementioned techniques are designed in GF 65 nm CMOS process, it is applicable to other silicon based technologies such as SiGe BiCMOS or SOI.

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