# Miniaturized 40–60 GHz On-Chip Balun With Capacitive Loading Compensation

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***Abstract*— A millimeter-wave balun by using the broadside-coupled transmission lines and capacitive loading compensation is proposed and investigated. The balun is designed and verified by using a commercial SiGe BiCMOS technology. The measured results show that in the frequency range of 40–60 GHz, the amplitude mismatching and absolute phase error are less than 0.2 dB and 2.7°, respectively. The compact size of the balun is only 200 $\mu$m × 180 $\mu$m including grounding shield.**

***Index Terms*— SiGe BiCMOS, millimeter-wave, balun, multi-layer, RFIC, pattern ground, capacitive loading compensation (CLC).**

## I. Introduction

THE recent significant progress of the silicon based IC technologies such as SiGe BiCMOS and CMOS makes them alternative solutions for millimeter-wave circuits and system. The challenges for BiCMOS/CMOS RF front end design are to combat the high losses from the substrate and the high resistivity metal [1]–[4]. In order to reduce the substrate loss and common mode noise, differential architectures are wildly used in wireless communication [5]–[7] especially in high data rate communication system. Therefore, a balun is required to provide balanced differential outputs from the single-ended input signal. There are numerous publications on balun designs in the literatures [1]–[7]. The on-chip balun with larger size is firstly implemented on a non-commercial high-resistivity silicon process. A multilayer symmetrically stacked balun by using symmetric magnetic coupling is implemented on a standard commercial CMOS [2]. The general 3D stacked transformer/balun is thoroughly investigated and developed with compact size below 10 GHz. A transmission line compensation technique [4] is proposed to reduce the imbalance of a Marchand balun due to the unequal odd- and even-mode phase velocities of the coupled lines. A novel off-chip branched line balun based on right/left transmission lines is developed in [5] with good performance but large size. A novel balun by adding a shunt susceptance between the two couplers of the Marchand balun to adjust in the phase balance is introduced in [6]. A CMOS 77GHz bandpass filter with balanced outputs or filtering balun is proposed in [7].

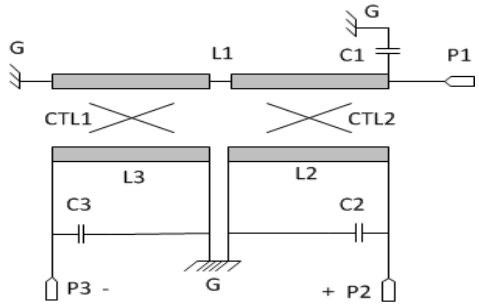


Fig. 1. General balun topology with capacitive loading compensation.

In this letter, a novel balun architecture by using proposed capacitive loading compensation (CLC) is introduced for the balun with compact size and good balance characteristics. The proposed balun is designed and verified by using a commercial 1P6M BiCMOS technology. The measurement results of the compact balun show that the operation bandwidth can cover the frequency range from 40GHz to 60GHz with the amplitude mismatching of less than 0.2 dB and absolute phase error of less than 2.7 degrees.

## II. Balun With Compensation

The simplified transmission line model of the proposed balun architecture is shown in Fig. 1. Coupled transmission lines (CTL) i.e. CTL1 and CTL2 are designed with strong coupling coefficient by using the broadside coupling [8]. The proper grounding (G) at one end of L1 and common grounding (G) shared by of L2 and L3 is set for the balun operation with the basic amplitude and phase relationship. The capacitor C1 is purposely added in shunt in input port of P1, while capacitors C2 and C3 are connected in shunt in port P2 and P3 respectively. These capacitors have three functions: adjust matching for corresponding port, perform capacitive loading to reduce the transmission line lengths of L1 $\sim$ L3 for compact size and also adjust the phase and amplitude balance of the balun. Under lossless condition, this three-port balun with port definition given in Fig. 1, can be represented by its' optimum three-port matrices in Equation (1)

$$S_{balun} = \begin{bmatrix} 0 & \frac{j}{\sqrt{2}} & \frac{-j}{\sqrt{2}} \\ \frac{j}{\sqrt{2}} & \frac{1}{2} & \frac{1}{2} \\ \frac{-j}{\sqrt{2}} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (1)$$

The balun is matched at the input and has the power transmission coefficients of 3 dB (named theoretical 3dB loss) to the

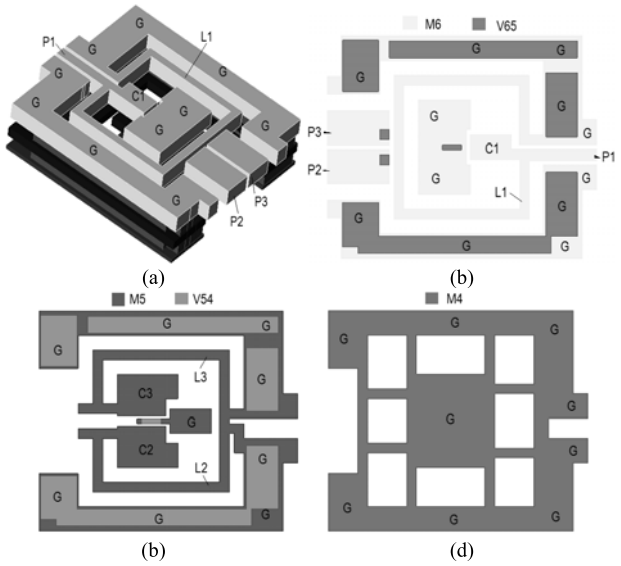


Fig. 2. The proposed CLC balun on the 1P6M BiCMOS process. (a) 3D View. (b) M6 and V65. (c) M5 and V54. (d) M4.

two output ports, where the signals are equal in amplitude but opposite in phase. For on-chip balun, the loss, size and balance are three key parameters for the implementation of the balun on lossy silicon substrate (with resistivity of $\sim$10$\Omega$/square) and thin metal layer with larger resistivity.

## III. Balun Design on IC Process

The proposed CLC 3D balun, based on the proposed balun architecture in Fig. 1, is shown in Fig. 2. It is constructed on a commercial 0.18 $\mu$m SiGe BiCMOS 1P6M process with six metal layers (M1 $\sim$ M6) from Tower Jazz Semiconductor Manufacturing. The thickness of the M6 is around 2.85 $\mu$m and the thicknesses of other layers are around 0.57 $\mu$m. The total thickness of inter-metal dielectric (IMD) layers is 10 $\mu$m. The thickness of silicon substrate is 280 $\mu$m. Vias (metal vias including V65 and V54) in Fig. 2 are used as interconnects among M6, M5 and M4, while "G" denote the metal or vias connected to ground. The primary coplanar waveguide line L1 together signal layer of C1 is built by using M6 layer as in Fig. 2(b). The secondary coplanar waveguide lines L2 and L3 together with the signal layer of compensation capacitors C2 and C3 are on metal layer M5 as in Fig. 2(c). With consideration of the lossy silicon substrate, the pattern ground layer to reduce the substrate loss and provide grounding, is built in metal layer M4 as given in Fig. 2(d), which has smaller substrate loss as compared to M1 $\sim$ M3. The common "G" ends of L2 and L3 opposite port 2 (P2) and port 3 (P3) while close to port 1 (p1) side are connected to ground. One end of L1 opposite to P1 is shorted to the ground guiding ring. The ground guiding ring surrounding L1, L2 and L3 denoted with "G" is connected together using via interconnects i.e. V65 and V54 among different metal layers from M4 to M6. It needs to be noted that C1 is self-designed by using metal-insulator-metal (MIM) type through metal plates in M6 and M5 and calculated as $C_1 = \frac{\varepsilon_0 \varepsilon_r W_{c1} L_{c1}}{d_{65}}$, while C2 and C3 are designed based on the Sandwich capacitors or (MIMIM) [8]

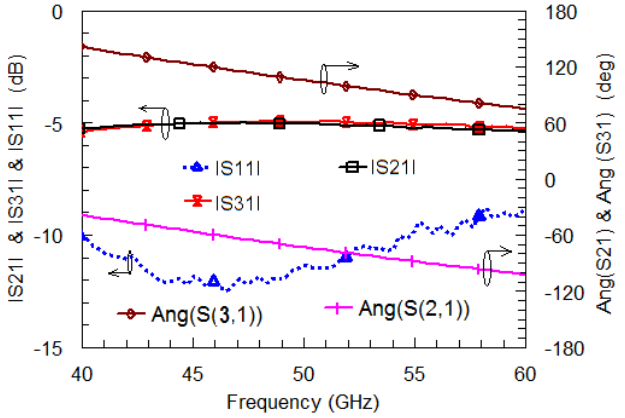


Fig. 3. The measured characteristics of the CLC balun.

by using M6, M5, and M4 with signal layer on M5. It can be calculated by using Equation (2)

$$C_{2/3} = \frac{\varepsilon_0 \varepsilon_r W_{c2/c3} L_{c2/c3}}{d_{65}} + \frac{\varepsilon_0 \varepsilon_r W_{c2/c3} L_{c2/c3}}{d_{54}} \quad (2)$$

where $d_{65}$, and $d_{54}$ are the substrate thicknesses between the layers of M6 and M5 and the layers of M5 and M4 respectively. $W_{ci}$ and $L_{ci}$ ($i$ = 1, 2 or 3) are the effective metal widths and lengths for the capacitor $C_i$. The circuit simulator and EM simulator from ADS are used to design and optimize the proposed 3D balun. Firstly, the transmission line S-parameters from EM simulation and ideal values of capacitors are used to determine the initial lengths of the lines and the dimensions of capacitors. Then the ideal capacitors are replaced by using one port S-parameter of the electromagnetic results of the MIM and Sandwich capacitor structures. The designed parameters/dimensions are given as follows: $\varepsilon_r$ = 4.2, $d_{65}$ = 2 $\mu$m, $d_{54}$ = 2 $\mu$m, L1 = 430 um with $W_{c1}$ = 8 um, L2 = L3 = 205 um with $W_{c2} = W_{c3}$ = 8 um, the MIM cap $C_1$ = 11.2 fF with size of $L_{c1}$ = 30 um, $W_{c1}$ = 20 um, MIMIM cap C2 = C3 = 51.5 fF with size of $L_{c2}$ = 42 um, $W_{c2}$ = 33 um, and $L_{c3}$ = 42 um, $W_{c3}$ = 33 um respectively. To further evaluate the CLC effect on balun, two balun structures with the same parameters/dimensions except one with capacitors and the other without capacitors are evaluated by using EM simulator. It is found that the balun structure without capacitors C1, C2 and C3 operates in the center frequency of 70GHz with imbalance of 1dB in amplitude and 3degrees in phase and return loss of 6 dB, while the balun structure with capacitors C1, C2 and C3 operates in the center frequency of 51 GHz with imbalance of only 0.05 dB in amplitude and 0.3 degrees in phase and return loss of 9.7dB. It can be seen from the investigation that the CLC has functions of matching adjustment, frequency down shifting (means size reduction under the same operating frequency) and balance adjustment.

## IV. Results and Discussion

The balun structure with CLC is fabricated. On-chip measurement is carried on by using the Agilent four-port network analyzer PNA-X together with Cascade Probe Station.

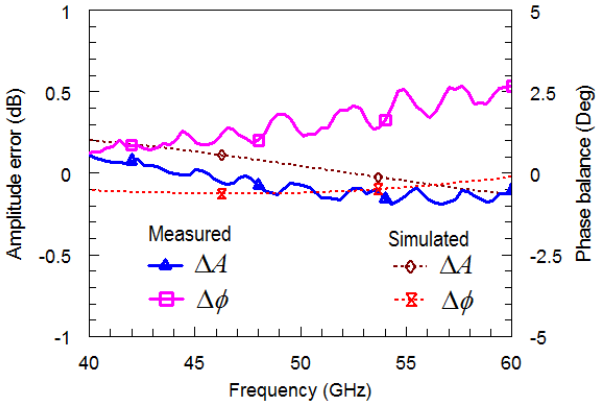


Fig. 4. Comparison of the measurement and simulation results.

TABLE I

COMPARISON OF THE BALUN CHARACTERISTICS

| Ref | Freq. (GHz) | Phase Err (deg) | Size (um$^2$) | *IL dB | Amp Err (dB) |
|---|---|---|---|---|---|
| [1] | 1.6~2.6 | <2 | 2300X1200 | -1.3 | <0.3 |
| [2] | 0.8~2.5 | <3.2 | 270X270 | -3 | <0.4 |
| [3]* | 10~70 | <±5 | N.A. | -0.7 | <±1 |
| [4] | 45~75 | N.A. | 210X36 | <-3 | N.A. |
| [5] | 0.9~2.1 | <±3 | 29000X30500 | -0.6 | <1 |
| [6] | 7~11 | N.A. | 750X800 | -3 | <0.3 |
| [7] | 75~85 | <±4 | 550X700 | -3 | <1.4 |
| **This work** | **40~60** | **<2.7** | **200X180** | **-1.9** | **<0.2** |

* IL is the loss value excluding 3dB theoretical loss

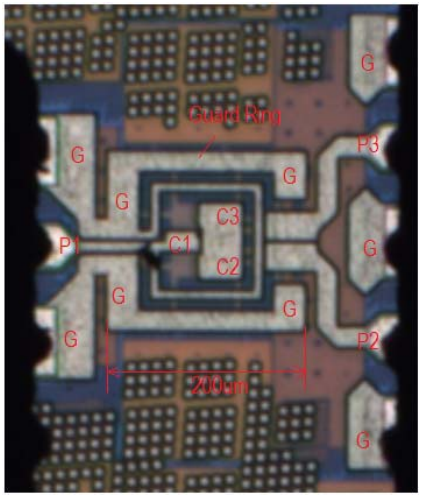


Fig. 5. Die photo of fabricated CLC balun.

The measured three-port results of the CLC balun are shown in Fig. 3. From 40GHz to 60GHz, the measured input return loss is better than 9dB and the measured $|S_{21}|$ and $|S_{31}|$ in dB are 4.9 ~ 5.3dB and 5.0 ~ 5.4dB respectively including the input/output PAD loss of about 0.4dB at 60 GHz. To characterize the balun balance, the amplitude imbalance is expressed in terms of the insertion loss of two outputs ($S_{21}$ and $S_{31}$) on logarithmic scales as Equation (3)

$$\Delta A = |S_{21}|_{dB} - |S_{31}|_{dB} = \log \left| \frac{S_{21}}{S_{31}} \right| \quad (3)$$

For conveniently evaluating the phase errors in a balun device, the phase imbalance is characterized using the phase difference with reference to 180 degrees as Equation (4)

$$\Delta\phi = \angle S_{21} - \angle S_{31} + 180^\circ \text{ (Degrees)} \quad (4)$$

The measured results of the phase and amplitude imbalance are given in Fig. 4. Good phase accuracy of less than 2.7 degree and amplitude accuracy of less than 0.2 dB, as compared with the state of the arts in Table I, are achieved. The core die size of the balun, as shown in Fig. 5, is only 200 $\mu$m × 180 $\mu$m including grounding shield.

## V. CONCLUSION

A novel miniaturized millimeter-wave balun using the CLC approach with self-built capacitors is proposed and verified by on a commercial SiGe BiCMOS technology. The fabricated balun demonstrates good balance characteristic, insertion loss and compact size. The approach of CLC can achieve good performance and give more flexibility for balun design. The implemented miniaturized balun provides 20GHz bandwidth centered in 50GHz with good balance characteristics for millimeter-wave applications.

## ACKNOWLEDGMENT

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