Coupled Dual LC Tanks Based ILFD With Low Injection Power and Compact Size

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***Abstract*—This letter presents a fully differential injection locked frequency divider using coupled dual LC tanks. The proposed injection locked frequency divide-by-2 divider achieves a wide locking range with low injected power levels. The divider, fabricated in 0.18 μm SiGe BiCMOS process achieves a locking range of 3.77 GHz with an injected power as low as -16 dBm, a phase noise of -116 dBc/Hz at 10 kHz offset with an input referred phase noise of -109.7 dBc/Hz at 10 kHz offset at 25 GHz, maximum output power of -2.44 dBm, efficiency of 18.5% and the dc power consumption is 4.8 mW.**

***Index Terms*—Coupled dual LC tanks, divide-by-2, injection locked frequency divider (ILFD), K-band, 24 GHz.**

I. Introduction

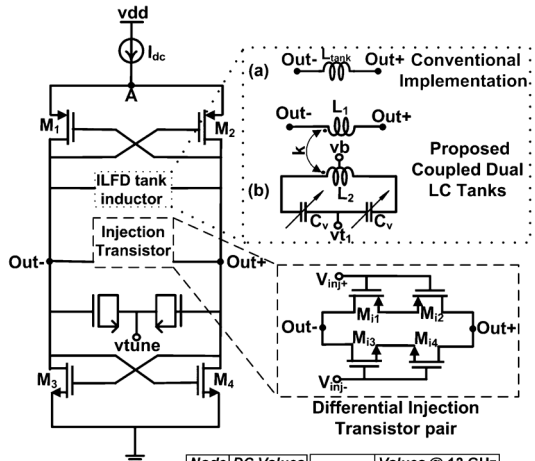
FREQUENCY dividers, following the voltage controlled oscillator (VCO), are important building block especially for frequency synthesizers operating in K-band and beyond. In the frequency range of K-band and above, injection locked frequency divider (ILFD) is preferred for its low voltage and lower power consumption over the common-mode logic (CML) dividers but it has a narrow locking range as compared to CML divider. Many techniques have been proposed to improve the locking range of ILFD [1]–[9]. Dual band ILFD is reported in [1], [2] but the reported locking range in each band is small. Improved locking range with switched inductor and inductor based injection enhancement is reported in [3]–[6] but chip area is increased due to additional inductors. In [7] the locking range is extended with direct and tail current injection but has insufficient output power that is needed to drive the subsequent blocks. In [8], [9] locking range is increased by coupling two ILFD cores with a coupling circuit but requires more area.

In a typical low power transceiver, the input power to the ILFD can be much less than -10 dBm due to the low output power of VCO for power saving together with the interconnect loss. In such cases, the ability of ILFD to operate with low injected power levels and deliver higher power efficiency (P_{out}/P_{DC}) is an important requirement for integration into the transceiver. The locking range of the ILFD is given by

$$\frac{\Delta\omega}{\omega_o} = \frac{I_{inj}}{2Q \times I_{OSC}}. \quad (1)$$

From (1), to achieve a wide locking range at low injection levels (I_{inj}), either the quality factor of the ILFD tank or the oscillator core current (I_{osc}) has to be decreased which is contrary to the requirement for high power efficiency.

Therefore, in this work, the focus is on increasing the locking range of the ILFD with low injected power levels while keeping a low phase noise and high power efficiency simultaneously. With the adoption of the proposed coupled dual LC tanks together with differential injection transistor pairs, the proposed ILFD exhibits an excellent tradeoff amongst the above design aspects simultaneously.



Device	Design Values
M_1,M_2	100 µm /0.18 µm
M_3,M_4	60 µm /0.18 µm
M_{i1}-M_{i4}	35 µm /0.18 µm

Node	DC Values
vdd	1.8 V
Out	0.65 V
V_{inj}	1.3 V
vb	0.9 V

	Values @ 12 GHz
L_1	300 pH
L_2	100 pH
QL_1,QL_2	15,10.7
k	0.73

Fig. 1. Schematic of injection locked divide-by-2 divider.

II. Circuit Design of ILFD

The schematic of the proposed ILFD with coupled dual LC tanks is shown in Fig. 1. The coupled dual tanks of the proposed ILFD is formed by the coupled inductors L_1 and L_2 together with the variable capacitance Cv implemented by using digital tuning bit. The transistors M_1 to M_4 provide the required negative resistance to compensate the tank losses. For a differential operation, differential injection transistor pairs using M_{i1} to M_{i4} is adopted. To reduce noise from the biasing circuit, the PMOS current mirror is chosen for better transistor flicker noise.

To derive the locking range, the ILFD in Fig. 1, is split into its equivalent AC half circuit as shown in Fig. 2(a). Since the source terminals of the PMOS cross-coupled transistors

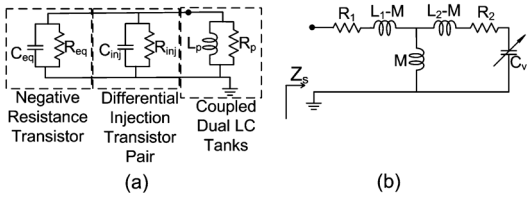


Fig. 2. Equivalent circuit (a) ILFD AC half circuit and, (b) series equivalent of coupled dual LC tank.

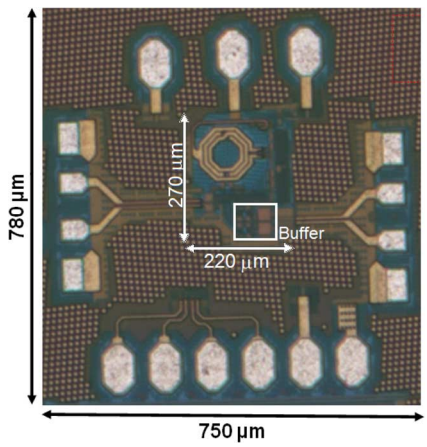


Fig. 3. Die microphotograph of ILFD.

are at AC ground (Node A in Fig. 1), the negative resistance transistors can be simply represented as parallel combination of R_{eq} and C_{eq}, where R_{eq} represents the equivalent negative resistance generated by the cross-coupled transistors and C_{eq} is the overall parasitic capacitance including the drain-source (C_{ds}) and the gate-source capacitances (C_{gs}) of the negative resistance transistors. The differential injection transistor pairs are simplified as shunt capacitance C_{inj} and channel resistance R_{inj}. The coupled dual LC tank is simplified into its parallel equivalent with L_p representing the equivalent inductance and R_p representing the overall resistive loss. As shown in Fig. 2(b), based on the T-model presented in [10], the series impedance of coupled dual LC tanks can be derived as $Zs = R_s + j\omega L_s$, where R_s and L_s is given by

$$R_s = R_1 + \frac{\omega^2 M^2 R_2}{[\omega L_2 - (\omega C_v)^{-1}]^2} \text{ and } L_S = L_1 + \frac{\omega^2 M^2 C_v}{1 - \omega^2 L_2 C_v}. \quad (2)$$

Using (2), the series impedance of coupled dual LC tanks can be represented in shunt as shown in Fig. 2(a), where, $R_p = R_s(Q'^2 + 1)$, $L_p = L_s(Q'^2 + 1)/Q'^2$ and $Q' = R_p/\omega L_p = \omega L_s/R_s$. Assuming a fixed oscillation frequency and high quality factor for capacitors and varactors, the quality factor of the ILFD is

$$Q = \frac{R_p // R_{inj}}{\omega L_p} \quad (3)$$

where $R_{inj} = (\mu_n C_{ox}(W/L)_n.(V_{GS} - V_{thn}))^{-1} \| (\mu_p C_{ox}(W/L)_p.(V_{SG} - |V_{thp}|))^{-1}$.

From Fig. 1, it can be observed that the source node of injection transistors is at AC ground and the injection current can be expressed as the function of transconductance of the injection transistor and its gate source voltage given by

$$I_{inj} = g_{m,inj} v_{gs,inj} \approx g_{m,inj} V_{inj}(t) \quad (4)$$

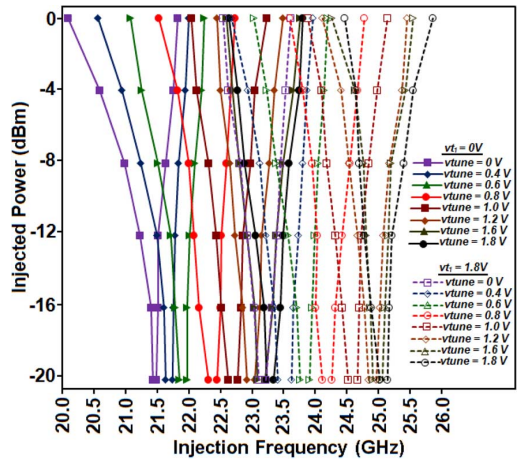


Fig. 4. Measured input sensitivity of ILFD.

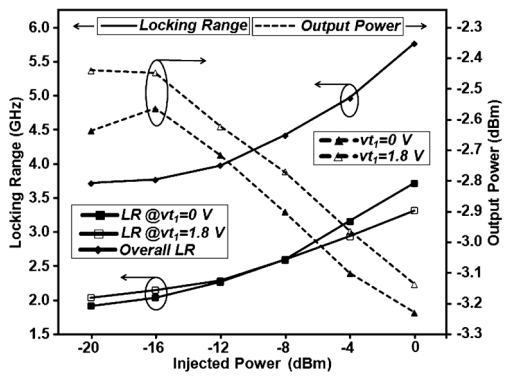


Fig. 5. Measured locking range and output power.

where, $g_{m,inj}$ is the transconductance of the injection transistor and $V_{inj}(t) = V_i \sin(\omega_i t)$, V_i being the incident amplitude, ω_i the incident frequency equal to $2\omega_o$. The oscillation current is

$$I_{osc} = g_{m,osc} v_o \approx g_{m,osc} \frac{I_{dc} R_{inj}}{2} \quad (5)$$

where, $g_{m,osc}$ is the oscillator transconductance represented by the cross-coupled transistors $M_1 - M_4$, v_o is the output voltage which is approximately dependent on the bias current I_{dc} and resistance of injection transistor R_{inj}. It should be noted that the approximation for v_o is valid only if R_p is larger than R_{inj}. Substituting (3), (4) and (5) into (1), the locking range of the ILFD considering the magnitude of $V_{inj}(t)$ is given by

$$\frac{\Delta\omega}{\omega_o} = \frac{g_{m,inj} V_i . \omega L_p}{g_{m,osc} I_{dc} R_{inj}^2}. \quad (6)$$

From (6), it can be seen that for low injection amplitudes (V_i), the locking range of the ILFD can be enhanced by (a) small bias current (I_{dc}), (b) a higher tank inductance and (c) the size of the injection transistors. Since the minimum required bias current is determined by the tank losses, minimum output power and required phase noise, in the proposed ILFD, the locking range is enhanced by using large tank inductance and increased width for differential injection transistor pairs. In comparison to the conventional implementation, the use of proposed coupled dual LC tank in the ILFD achieves a larger effective inductance due to the strong magnetic coupling between the coils with reduced effective chip area. With the differential injection transistor pair as injection transistors, (a) the ILFD realizes a fully differential

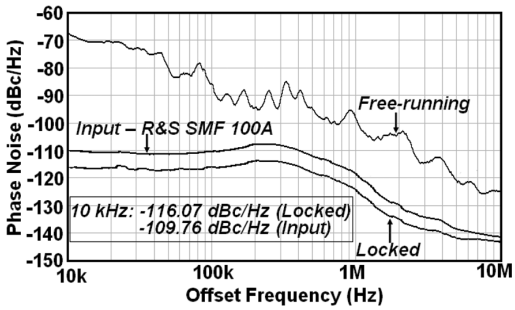


Fig. 6. Measured ILFD phase noise.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF ILFD PERFORMANCE

Ref.	**This Work**	[4]	[6]	[7]	[8]	[9]
F_{center} (GHz)	**24**	23	23	28	20	20
LR (%) @						
Pin = -10 dBm	**17.16**	-	15.7	10.88	-	-
Pin = -5 dBm	**18.49**	10.62	17.8	13.55	7.06	12
Pin = 0 dBm	**25.07**	11.76	23.7	21.47	13.08	16
P_{DC} (mW)	**4.8**	4.32	1.5	1.8	1.51	6.4
Vdd (V)	**1.8**	1.2	1.5	1.8	0.8	1.2
PN (dBc/Hz)						
@ 10 kHz	**-116**	-110	-110	-105	-108	-108
@ 1 MHz	**-125**	-	-131	-124	-123	-126
P_{out} (dBm)	**-0.5**	-	-11	-14	-8	-1
P_{out}/P_{DC} (%)	**18.56**	-	5.29	2.21	10.5	11.06
FOM (%/mW^2)						
Pin = -10 dBm	**6.63**	-	5.55	1.33	-	-
Pin = -5 dBm	**1.79**	-	1.75	0.52	1.55	0.65
Pin = 0 dBm	**0.97**	-	0.83	0.26	0.90	0.27
Area (mm^2)	**0.22 × 0.27**$^{\#}$	0.7 × 0.7	0.5 × 0.43$^{\#}$	0.83 × 0.54	0.36 × 0.64$^{\#}$	0.33 × 0.08$^{\#}$
Process Technology	**CMOS in 0.18µm SiGe**	90 nm CMOS	0.18µm CMOS	0.18µm CMOS	0.13µm CMOS	90 nm CMOS

$FOM = (LockingRangein\%/P_{in} \cdot P_{DC})(P_{out}/P_{DC})$, $^{\#}$—Core area

operation and (b) the series connection of injection transistor pairs has an increased transconductance thus providing a higher closed loop gain and a wider locking range with reduced total parasitic capacitance [11].

III. EXPERIMENTAL RESULTS

The proposed ILFD is implemented in Tower Jazz 0.18 μm SiGe BiCMOS process and the measurement is carried via on-wafer probing. The ILFD and buffer occupies a chip area of only 220 μm × 270 μm including the transformer core of 123 μm × 123 μm as can be seen from the die microphotograph in Fig. 3. The ILFD transformer is implemented in the topmost aluminium (Al) metal layer with a thickness of 2.81 μm and simulated using Agilent's Momentum EM simulations. With a supply voltage of 1.8 V, the ILFD core has a dc power consumption of 4.8 mW while the buffer consumes 3.8 mW. The measured input sensitivity and locking range of the ILFD is shown in Fig. 4 and Fig. 5 respectively. The ILFD measures a locked input frequency range from 21.41 to 25.18 GHz for −16 dBm input power and 20.09 to 25.86 GHz for 0 dBm input power. The measured output power of the ILFD under different injected power level is shown in Fig. 5. The ILFD measures a maximum and minimum output power of −2.44 dBm and −3.23 dBm respectively including the simulated buffer loss of 2.8 dB. The measured phase noise of ILFD is shown in Fig. 6. Under the locking condition at 25 GHz, the phase noise is −116.07 dBc/Hz at 10 kHz offset. Compared to the input signal generator phase noise of −109.76 dBc/Hz at 10 kHz offset, the achieved locked phase noise is better and close to the theoretical value of 6 dB as shown in Fig. 6. Table I lists the performance summary and comparison of the proposed ILFD with other ILFDs in the same frequency band. The proposed ILFD achieves a good power efficiency of around 18.56% excluding the buffer loss for the minimum output power. Considering power consumption and insertion loss of 50 Ω buffer following the ILFD, the power efficiency is 6.63%. The proposed ILFD is also fully differential ILFD with very compact size.

IV. CONCLUSION

In this letter, ILFD based on coupled dual LC tanks together with two differential injection transistor pairs to increase the locking range while maintaining a high quality factor is presented. With the presented technique, the implemented ILFD can achieve a wide locking range at low injected power levels and higher power efficiency. With a compact silicon area and fully differential design, the ILFD can be readily integrated with low power VCOs.

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