2.3 A 130-to-180GHz 0.0035mm^2 SPDT Switch with 3.3dB Loss and 23.7dB Isolation in 65nm Bulk CMOS

Fanyi Meng[1], Kaixue Ma[1], Kiat Seng Yeo[1,2]

[1]Nanyang Technological University, Singapore, Singapore,
[2]Singapore University of Technology and Design, Singapore, Singapore

Single-pole double-throw (SPDT) switches are a key building block for enabling transceiver time-division duplexing (TDD) when operated as a T/R switch or for eliminating imager fluctuations when operated as a Dicke switch. To provide acceptable compromises of NF, P_{out} and sensitivity in transceivers or imagers, the switches are required to feature an insertion loss of ~3dB and an isolation of ~20dB. Recently, mm-Wave/sub-mm-Wave transceiver and imager integrated circuits have gradually migrated to silicon platforms for low-cost consumer markets [1,2]. However, the associated SPDT switches operating beyond 110GHz are developed using advanced SOI or SiGe HBT technologies [3,4] and rarely implemented in CMOS due to the lossy substrate and poor transistor characteristics [2,5].

In the past decades, the mostly adopted topology to realize mm-Wave SPDT switches is to use impedance-inverting $\lambda_g/4$ transmission line (T-line) and shunt SPST cells as shown in Fig. 2.3.1, where λ_g is the guided wavelength [2-5]. The major issue of this topology is the bulky size of the $\lambda_g/4$ T-line that makes SPDT switches a costly solution. Besides, the pre-matching method of $\lambda_g/4$ T-line and SPST cells seems unnecessary to provide an internal 50Ω impedance matching between them. For example, a typical CPW line has insertion loss of ~1dB/mm at 110GHz, while the passive network used in matching SPST cells to 50Ω often causes more loss than the $\lambda_g/4$ T-line does [3]. Thus, it is challenging to design SPDT switches above 100GHz in CMOS using the conventional topology. In this paper, a new SPDT topology using a magnetically switchable artificial resonator is reported. The proposed resonant structure alleviates the problematic $\lambda_g/4$ T-line and matching networks, while its magnetic switching capability improves the switch isolation at zero compensation of insertion loss. The implemented switch achieves excellent performance from 130 to 180GHz and a remarkable size reduction of >96.5% compared to prior works [2-5].

Figure 2.3.1 shows the topology and configuration of the proposed SPDT switch. The switch comprises of 3 main coupled lines on thick copper layer OI (in grey) with switch transistors $M_{1,2}$ for providing the SPDT function, and 2 auxiliary coupled lines (in yellow) on the EA layer with switch transistors $M_{3\text{-}6}$ to switch the magnetic coupling strength between adjacent main coupled lines for isolation enhancement. The ground plane is formed with overlapped metal 1 and metal 2 with via connections to minimize the sheet resistance within the density rule allowance of the used process. In the operation mode where V_1 = 0V and $V_2 = V_{DD}$, M_1 is turned off to be treated as an off capacitance C_{OFF}, serving as part of the artificial resonator to provide simultaneous maximum power transfer from Port 1 to Port 2 and impedance matching to 50Ω. In this mode, transistor M_2 is turned on and has a small on resistance R_{ON} that effectively performs signal isolation from Port 1 to Port 3. The opposite operation mode follows the same operation mechanism.

Figure 2.3.2 illustrates the operation mechanisms of auxiliary coupled lines and switch transistors $M_{3\text{-}6}$. As the SPDT is symmetrical with respect to the center coupled line, the left half circuit is plotted in 2 operating states. In the state when V_a = 0V, auxiliary switch transistors $M_{3\text{-}4}$ are turned off. By properly selecting transistors $M_{3,4}$, the effective magnetic coupling coefficient between the main coupled lines $k_{1,2\text{-eff}}$ remains about the same. In the state when $V_a = V_{DD}$, transistors $M_{3\text{-}4}$ are turned on. For small R_{ON}, the effective magnetic coupling coefficient $k'_{1,2\text{-eff}}$ is reduced approximately by the product of the coupling coefficients between the main and auxiliary coupled lines. The right half circuit has the same operation mechanism. It is verified in simulation that $k_{1,2} = k_{1,3}$ = 0.442, $k_{1,2\text{-eff}} = k_{1,3\text{-eff}}$ = 0.441 and $k'_{1,2\text{-eff}} = k'_{1,3\text{-eff}}$ = 0.352. Thus, the auxiliary switches "off" state with strong effective magnetic coupling between main coupled lines can be used in the operation mode when signal "on" path is desired, while the auxiliary switches "on" state with weak magnetic coupling reduces the signal coupled through and hence is selected for better isolation. Figure 2.3.2 also shows one of the switch operation modes when Port 2 is the signal port and Port 3 is the isolation port. The artificial resonator is symmetrical and designed to resonant at around 150GHz. Stronger coupling from Port 1 to Port 2 and weaker coupling from Port 1 to Port 3 are achieved by auxiliary coupled lines and switch transistors $M_{3\text{-}6}$.

Figure 2.3.3 shows the small-signal equivalent circuit model for the proposed switch in the above-mentioned operation mode. All parameter values can be extracted using full-wave electromagnetic (EM) simulations, including self-inductances $L_{1\text{-}3}$, parasitic resistances $R_{1\text{-}3}$ and capacitances $C_{1\text{-}3}$ of each of the coupled lines. The optimized design parameters are listed in Figure 2.3.1, by using EM and circuit simulation with considerations of the metal dummy-fill effects. The switch transistors selected have R_{ON} of 5.72Ω and C_{OFF} of 25.7fF at 150GHz. The $R_{ON}\times C_{OFF}$ product calculated as 147fs for the used process is much worse than the SOI and SiGe HBT processes [3,4], and contributes the majority of switch insertion loss. However, the proposed artificial resonator structure causes only 0.6dB loss due to its compact size and low parasitic components.

Figure 2.3.7 shows the micrograph of the prototypes fabricated in a 65nm CMOS process. The Switch A is the proposed magnetically switchable artificial resonator switch as configured in Figure 2.3.1. The Switch B, by removing the auxiliary coupled lines and their connected transistors $M_{3\text{-}6}$, is used for comparison and verification on the advantages of the magnetic switching capability. The active area of the chip, including the low metal dummy-fill area, occupies only 0.0035mm^2. Two-port S-parameter measurements are performed from 140 to 220GHz using an Agilent 67GHz PNA-X, a 140-to-220GHz VDI's extension module and Cascade WR-5 probes, while Port 3 is internally terminated with an on-chip 50Ω resistor. The system is calibrated using an SOLT probe-tip calibration on a Cascade ISS substrate. Therefore, the RF pad loss is included in the insertion loss measurements.

Figure 2.3.4 shows that the insertion loss and isolation of the switches agreed well with those of the simulations. The measured insertion losses of Switch A and Switch B are close, which indicates that the loss contributed from the auxiliary coupled lines and transistors $M_{3\text{-}6}$ is negligible. The measured Switch A has a minimum insertion loss of 3.3dB at 155GHz. The insertion loss curve is flat with value less than 4dB from 140 to 180GHz. The isolation of Switch A is enhanced by ~2dB as compared to Switch B, thanks to the magnetic switching capability. Switch A has measured isolation >21.8dB from 140 to 180GHz. From the simulation results and simple curve extrapolation, the fabricated Switch A is expected to achieve insertion loss better than 4dB and isolation better than 21.1dB in the 130-to-140GHz range, which is not covered due to measurement setup limits. Figure 2.3.5 shows the return loss and switching-speed performance. The return loss is >10dB from 130 to 180GHz. The simulated switching "on" and "off" times are 0.58ns and 0.53ns respectively, which could support Gb/s modulation and short-pulsed active radar applications. The SPDT switch has a simulated P_{1dB} of 11.4dBm at 155GHz. Figure 2.3.6 shows the performance comparison of this work with the state of the art. Compared to the switches in advanced SOI and SiGe HBT processes, the insertion loss and isolation of the proposed switch achieves comparable results to the state of the art. However, in the comparison table shown in Fig. 2.3.6, the proposed switch achieves the highest operating frequency in CMOS switches and smallest circuit size of 0.0035mm^2 that is only 1.5 to 3.5% of the size occupied in prior works [2-4].

Acknowledgement:
The authors would like to acknowledge VIRTUS in Nanyang Technological University for supporting this work and Mr. Lim Wei Meng for supporting chip measurement.

References:
[1] M. Boers, et al., "A 16TX/16RX 60GHz 802.11ad Chipset with Single Coaxial Interface and Polarization Diversity," *ISSCC Dig. Tech. Papers*, pp. 344-345, Feb. 2014.
[2] Z. Chen, et al., "A BiCMOS W-Band 2×2 Focal-Plane Array With On-Chip Antenna," *IEEE J. Solid-State Circuits*, vol. 47, pp. 2355-2371, Oct. 2012.
[3] M. Uzunkol and G. M. Rebeiz, "140-220 GHz SPST and SPDT Switches in 45 nm CMOS SOI," *IEEE Microwave and Wireless Component Letters*, vol. 22, pp. 412-414, Aug. 2012.
[4] A. C. Ulusoy, et al., "A Low-Loss and High Isolation D-Band SPDT Switch Utilizing Deep-Saturated SiGe HBTs," *IEEE Microwave and Wireless Component Letters*, vol. 24, pp. 400-402, June 2014.
[5] M. Uzunkol and G. M. Rebeiz, "A Low-Loss 50-70 GHz SPDT Switch in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, pp. 2003-2007, Oct. 2010.

Figure 2.3.1: Conventional SPDT topology and proposed SPDT topology and configuration.

Figure 2.3.2: Operating mechanisms of auxiliary coupled lines with switch transistors $M_{3\text{-}6}$ and the SPDT switch in one operation mode.

Figure 2.3.3: Equivalent small-signal circuit model in operation mode as in Figure 2.3.2 and insertion-loss contribution chart.

Figure 2.3.4: Insertion loss and isolation performance of the SPDT switches.

Figure 2.3.5: Return loss and simulated switching speeds.

	[5] JSSC 2010	[2] JSSC 2012	[4] MWCL 2014	[3] MWCL 2012	This Work
Technology f_T (GHz)	90nm CMOS 130	0.18µm SiGe BiCMOS 200	0.13µm SiGe HBT 300	45nm SOI 485	65nm Bulk CMOS 220
Transistor $R_{ON}\times C_{OFF}$ (fs)	180	132	83.7	75.6	147
Frequency (GHz)	50-67	75-110	96-163	140-220	130-180
Insertion Loss (dB)	1.5-2 #	2.8-3.1 #	2.6-3	3-4.5	3.3-4
Return Loss (dB)	>8	>10	>10	>10	>10
Isolation (dB)	25-27.5	21-22	23.5-29	20-30	21.1-23.7
P_{1dB} (dBm)	13.5 †	Not Mentioned	17 @ 94 GHz	10 †	11.4 †
Size Excluding Pads (mm^2)	0.27	0.114	0.228	0.10	0.0035
Topology *	$\lambda_g/4$ TL + SS-SPST	$\lambda_g/4$ TL + SS-SPST	$\lambda_g/4$ TL + DS-SPST	$\lambda_g/4$ TL + DS-SPST	Magnetically Switchable Artificial Resonator

* TL: Transmission line; SS: Single-shunt; DS: Double-shunt
\# Pad loss de-embedded † Simulation

Figure 2.3.6: Comparison with state-of-the-art SPDT switches.

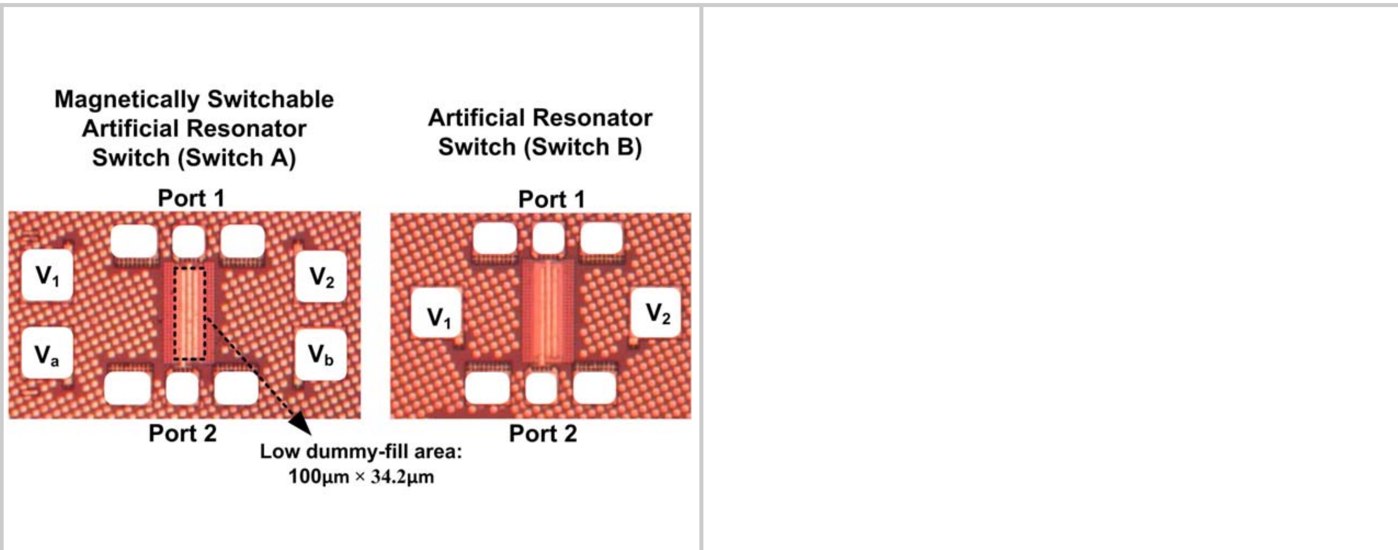

Figure 2.3.7: Die micrographs of fabricated switches.