2.5 A 2-to-6GHz Class-AB Power Amplifier with 28.4% PAE in 65nm CMOS Supporting 256QAM

Wanxin Ye[1], Kaixue Ma[1], Kiat Seng Yeo[1,2]

[1]Nanyang Technological University, Singapore, Singapore
[2]Singapore University of Technology and Design, Singapore, Singapore

Wideband power amplifiers (PAs) with high power-added efficiency (PAE) are required by software-defined radio and high-data-rate communications. A PA in Class-AB, which can provide linear amplification with PAE better than Class-A, has been reported in [1] to achieve bandwidth larger than one octave. However, Class-AB operation generates a large amount of 2nd-harmonic current at the transistor output, which has amplitude as high as up to 42% of the fundamental current in theory [2]. An output matching network, providing optimum load impedance only at the fundamental frequency, is insufficient to achieve good power performance, bringing big challenges to integrated Class-AB PA design with octave bandwidth. In this work, we demonstrate a 2-to-6GHz (fractional bandwidth of 115.5%) Class-AB PA designed in 65nm CMOS. An output matching technique based on differential architecture, which enables the PA to achieve a maximum PAE of 28.4% and an overall PAE above 19%, is proposed to provide transistor output with optimum load impedance for both fundamental and 2nd harmonic over an octave bandwidth. Without using any pre-distortion, the PA can deliver output power of 9.31 to 11.31dBm with EVM<-32dB for 256QAM signal (802.11ac format, 20MHz bandwidth) from 2 to 6GHz.

Figure 2.5.1 shows the schematic of the proposed PA. To design the output matching network, optimum load impedances for fundamental (Z_{opt_1st}) and 2nd-harmonic (Z_{opt_2nd}) frequencies of the output stage are simulated from 2 to 6GHz. A model composed of parallel R_{out} and C_{out} (27Ω and 0.94pF for the given device) showing good agreement with Z_{opt_1st} over the bandwidth is built for synthesizing the matching network for the fundamental frequency. With Z_{opt_1st} set at the fundamental frequency, simulated contours of P_{SAT} and PAE at representative frequencies of 2.4, 3.7 and 5.8GHz for load impedance at the 2nd harmonic are shown in Fig. 2.5.2, where impedances on the Smith chart are normalized to R_{out}. It shows that even with the fundamental frequency optimally matched, load impedance at the 2nd harmonic may vary P_{SAT} and PAE by 4.56/4.07/3.58dB and 29.6%/26.1%/21.1% respectively. Considering the susceptance of C_{out}, target areas of 2nd-harmonic impedance on the Smith chart indicate that impedance close to a short circuit, or capacitive impedance with normalized amplitude smaller than 1, is required at the current source reference plane of the transistor output to achieve good P_{SAT} and PAE.

To make the matching of the fundamental and 2nd harmonic over an octave possible, differential architecture is adopted such that fundamental currents at the transistor output are in differential mode but 2nd-harmonic currents are in common mode. By utilizing the coupling inside the transformer primary winding and the different behaviours of the transformer center-tap under the two modes, the output matching network providing Z_{opt_1st} and Z_{opt_2nd} with bandwidth larger than one octave can be designed. As shown in Fig. 2.5.1, the two halves of the transformer primary winding separated by the center-tap can be viewed as two coupled coils (L_{PH1}, L_{PH2}). Coupling between them (k_{12}) leads to equivalent inductance L_{DM} in differential mode for fundamental matching, and L_{CM} in common mode for 2nd-harmonic matching. For fundamental matching, a 3rd-order bandpass matching network with minimum reflection coefficient [3] is synthesized using 2.3 and 6GHz as the lower and upper band edges to ensure coverage of 2.4 and 5GHz ISM bands after fabrication. Norton transformations are performed such that a transformer with L_P=2.46nH, k=0.816 and n=0.826 is inserted into the matching network and the output is matched to 50Ω (Fig. 2.5.1). If the transformer center-tap is AC-grounded, the 1.49pF (0.94pF+0.55pF) capacitance on each primary port of the transformer used for fundamental matching will resonate in parallel with L_{CM} (0.41nH) at 6.44GHz (the 2nd harmonic of 3.22GHz), degrading power performance around 3.22GHz. To obtain capacitive impedance for the 2nd-harmonic frequency range of 4-to-12GHz, inductor L_{tap} (1.47nH) is inserted between the transformer center-tap and V_{DD} to reduce the parallel resonant frequency to below 4GHz. A trace width of 12µm is used for L_{tap} to reduce its parasitic resistance to only 0.55Ω at DC. A capacitor C_{tap}=0.5pF is then connected to the transformer center-tap such that impedances at the 2nd harmonic at the current source reference plane all have normalized amplitude smaller than 1. Parallel resonance, which will happen at the higher frequency end if C_{tap} is too large, should be avoided. Larger k_{12}, which can be obtained through multi-turn construction for the transformer primary winding, reduces the value of L_{CM} when a specific L_{DM} is required for fundamental matching, leading to larger achievable bandwidth for the 2nd-harmonic match. Because the transformer center-tap functions as a virtual ground in differential mode, L_{tap} and C_{tap} will not affect the matching for the fundamental. Figure 2.5.2 shows that with the designed matching network, load impedances at the 2nd harmonic in a wide frequency range are moved to the target area. Meanwhile, impedances at the current source reference plane are moved to an area close to a short circuit or being capacitive with normalized amplitude smaller than 1.

To support single-ended input, an active balun with a phase-error correction technique [4] is used as a driver stage to perform single-to-differential conversion at the PA input. All transistors in the balun are designed with the same size and same bias current. Simulated phase error maintains less than 0.5° from 2 to 6GHz when providing required driving power. With a small area of 0.13×0.13mm^2, the 2-stage structure of the active balun increases gain of the driver stage and reduces the input transistor size required to generate targeted driving power, allowing to use a single resistor of 70Ω as input match in a large bandwidth.

To reduce AM-PM distortion of the Class-AB PA, varactor-based capacitance compensation is used in the output stage. As shown in Fig. 2.5.3, different from PMOS transistors used conventionally [5], capacitance of a PMOS varactor is found to be more complementary to the cascode structure's input capacitance, which is affected by Miller effect and the input impedance of the common-gate device. A PMOS varactor with larger ratio of C_{max}/C_{min} also reduces the total capacitance after compensation, which is critical for the inter-stage matching network to achieve large bandwidth and good gain flatness. With the proposed compensation, the PA measures AM-PM distortion < ±2° up to P_{1dB} and gain flatness of ±0.8dB from 2 to 6GHz.

The PA is biased with DC current of 59mA from 1.8V for the driver stage and 23.6mA from 3.3V for the output stage. Figure 2.5.4 shows that from 2 to 6GHz the PA achieves S_{21} of 23.6±0.8dB and S_{11}<-11.8dB. Large signal measurement of the PA (Fig. 2.5.5) indicates a peak P_{SAT} of 22.4dBm at 2.8GHz and a peak PAE of 28.4% at 2.3GHz. Over the whole bandwidth, P_{SAT} and PAE remain above 20.1dBm and 19% respectively, and P_{1dB} is in the range of 17.81 to 20.73dBm (1.7 to 2.4dB lower than P_{SAT}). Compared to a counterpart without dedicated matching for the 2nd harmonic, the proposed PA improves P_{SAT}, P_{1dB} and PAE in a wide frequency range, with maximum improvements of 1.9dB, 2.0dB and 7.5% respectively. These maximum improvements are all observed at 3.1GHz, showing good agreement with analysis.

To verify the PA's capability of delivering modulated signals over the bandwidth, input signals with frame format of 802.11n (64QAM; 20 and 40MHz bandwidth) and 802.11ac (256QAM; 20, 40 and 80MHz bandwidth) with center frequency varied from 2 to 6GHz are amplified by the PA without using any pre-distortion. Output powers were recorded when EVM increased to -28dB for 64QAM and -32dB for 256QAM, and the results are shown in Fig. 2.5.6 and Fig. 2.5.7. An 802.11ac format signal with 160MHz bandwidth was not measured due to limitations of the signal generator used. The decreasing of output power as signal bandwidth increases is mainly due to the increased EVM of the input signal provided by the signal generator, which is around -40dB for a bandwidth of 20MHz and/or 40MHz, but around -36dB for 80MHz. Performances of the PA are summarized in Fig. 2.5.7, showing that the PA can support applications requiring linear amplification from 2 to 6GHz.

Fabricated in the same process, the PA and its counterpart each occupy an area of 0.57×1.57mm^2 including pads, as shown by micrographs in Fig. 2.5.7.

Acknowledgement:
The authors would like to thank VIRTUS (School of EEE, NTU) for supporting this work and Global Foundries for chip fabrication.

References:
[1] H. Wang, *et al.*, “A 5.2-to-13GHz Class-AB CMOS Power Amplifier with a 25.2dBm Peak Output Power at 21.6% PAE,” *ISSCC Dig. Tech. Papers*, pp. 44-45, Feb. 2010.
[2] S. C. Cripps, *RF power amplifiers for wireless communications*, Artech House, 2006.
[3] D. E. Dawson, “Closed-form solutions for the design of optimum matching networks,” *IEEE Trans. Microwave Theory and Techniques,* vol. 57, pp. 121-129, 2009.
[4] H.-H. Chiang, *et al.*, “A 90 nm CMOS V-band low-noise active balun with broadband phase-correction technique,” *IEEE J. Solid-State Circuits,* vol. 46, pp. 2583-2591, 2011.
[5] D. Chowdhury, *et al.*, “A Single-Chip Highly Linear 2.4GHz 30dBm Power Amplifier in 90nm CMOS,” *ISSCC Dig. Tech. Papers*, pp. 378-379, Feb. 2009.

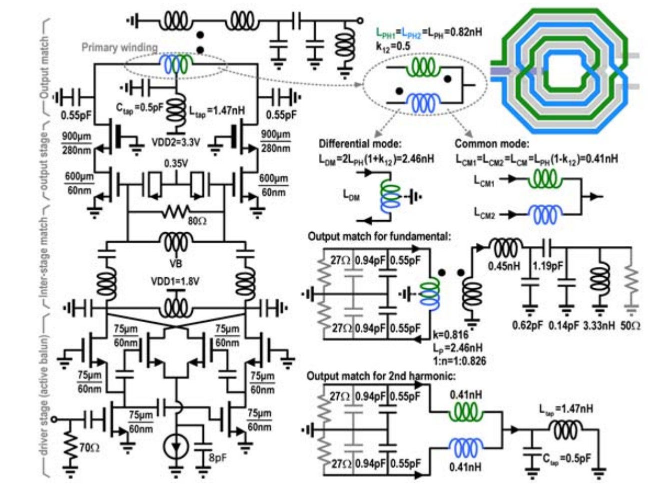


Figure 2.5.1: Schematic of proposed PA, transformer input inductance in differential mode and common mode, and equivalent circuit of output matching network for fundamental and 2nd harmonic.

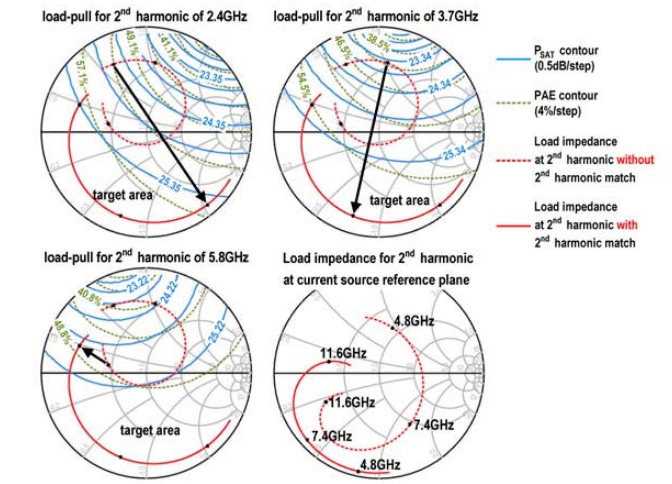


Figure 2.5.2: Load-pull simulation and load impedance for 2nd harmonic of representative fundamental frequencies in band.

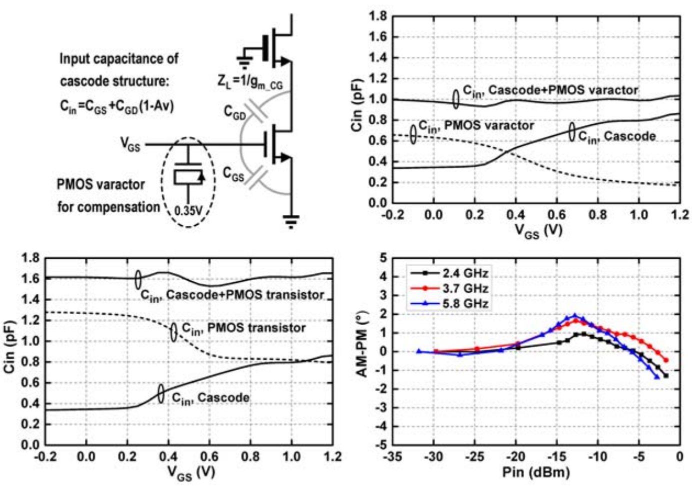


Figure 2.5.3: Input capacitance compensation of cascode structure based on PMOS varactor and measured AM-PM distortion of PA up to P_{1dB}.

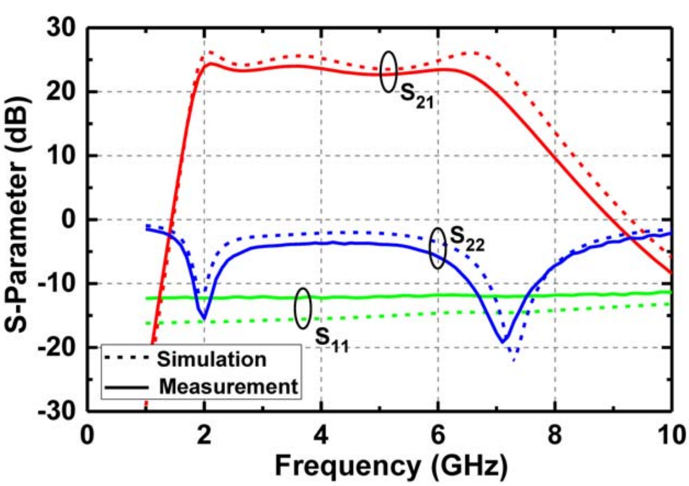


Figure 2.5.4: Simulated and measured S-parameters from 1 to 10GHz.

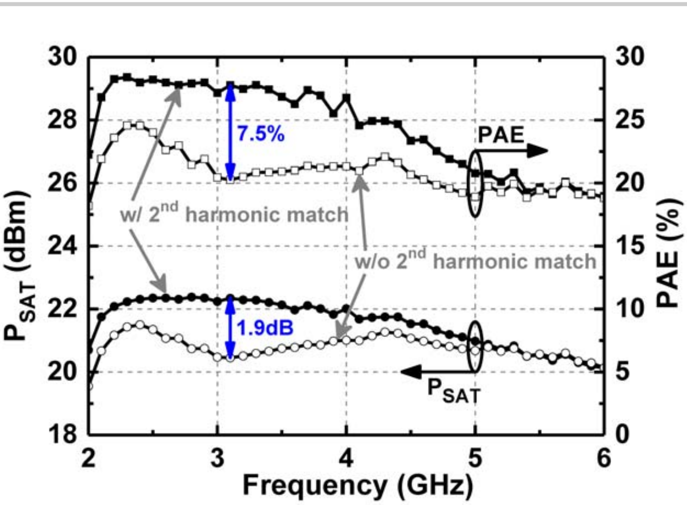


Figure 2.5.5: Measured P_{SAT} and PAE for the PA with 2nd-harmonic match and its counterpart without 2nd-harmonic match.

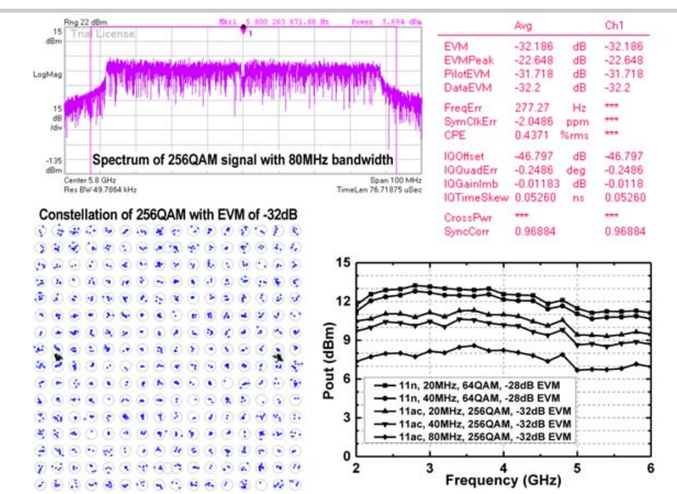
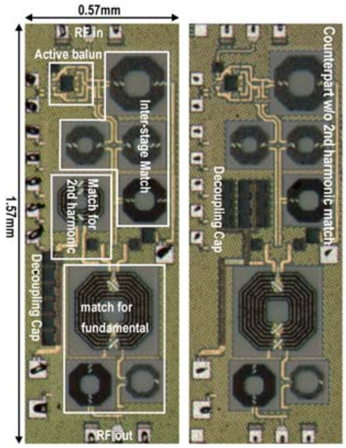


Figure 2.5.6: Measured output power for 64QAM (802.11n format) and 256QAM (802.11ac format) with EVM of -28dB and -32dB respectively. Spectrum and constellation are for 256QAM signal with 80MHz bandwidth at 5.8GHz.



	This work	Counter-part	Ref. [1] ISSCC 2010
Wideband 2nd harmonic match	**Yes**	No	No
Bandwidth (GHz)	2-6	2-6	5.2-13
FBW* (%)	115.5	115.5	94.9
Gain (dB)	23.6±0.8	23.5±0.9	18.5(peak)
P_{SAT} (dBm)	20.1-22.4	19.5-21.5	21.5-25.5
P_{1dB}(dBm)	17.8-20.7	17.8-19.5	22.6 (peak)
PAE (%)	19-28.4	18.2-24.6	11.5-21.6
AM-PM	<±2°	<±2°	-
$Pout^1$ (dBm)	11.12-13.24	10.72-12.16	-
$Pout^2$ (dBm)	10.66-12.80	10.27-11.93	-
$Pout^3$ (dBm)	9.31-11.31	8.64-10.34	-
$Pout^4$ (dBm)	8.52-10.63	8.04-9.57	-
$Pout^5$ (dBm)	6.69-8.59**	6.23-7.39**	-
Area (mm×mm)	0.57×1.57 (w/ pads)	0.57×1.57 (w/ pads)	0.45×1.55 (core)
Tech.	65nm	65nm	90nm

$Pout^1$: 802.11n format, 64QAM, 20MHz, EVM=-28dB

$Pout^2$: 802.11n format, 64QAM, 40MHz, EVM=-28dB

$Pout^3$: 802.11ac format, 256QAM, 20MHz, EVM=-32dB

$Pout^4$: 802.11ac format, 256QAM, 40MHz, EVM=-32dB

$Pout^5$: 802.11ac format, 256QAM, 80MHz, EVM=-32dB

*FBW: fractional bandwidth, calculated as $(f_H - f_L) / \sqrt{f_L \times f_H}$

**Limited by EVM of signal generator (-36dB)

Figure 2.5.7: Die micrographs and performance comparison.