

A hybrid CMOS Clock Divider for PLL of 60GHz Transceiver

*Yisheng Wang,
Nanyang Technological
University,
Yisheng@ntu.edu.sg*

*Kaixue Ma,
Nanyang Technological
Universit,
KXMA@ntu.edu.sg*

*Kiat Seng Yeo
Nanyang Technological
University,
EKSYEO@ntu.edu.sg*

Abstract

A hybrid multi-mode clock divider for PLL which used for 60GHz RF transceiver by using both integer-N and fraction-N structure is designed and implemented in this work. Full CMOS digital design is used to implement the circuit to achieve both low power and high flexibility. The digital clock divider includes high speed 3/4 dual modulus prescaler, a 24 modulus divider controller and 3 stage Delta-Sigma Modulator. The divider works up to 3.24GHz. The total power consumption is from 4mW to 9mW based on the different working modes. A MASH111 architecture is selected to implement the fraction-N divider.

1. Introduction

The 60GHz communication band is just released to consumer electronics to provide high speed giga-bits per second data transmission. Some standards are released already for this frequency band [1–3]. It is very important for the RF transceiver to fulfill those entire existing or coming standards, which has different channel definition on LO location, channel bandwidth, and reference clock frequency. A Phase Lock Loop (PLL) is widely used as a variable frequency source in modern radio transceivers. Programmable clock divider is employed within the loop to divide the VCO output frequency down to the reference frequency. The divider is one of the key components to provide the programmability of the frequency synthesizer by changing the divide rate.

The low power consumption is the key consideration for this work because the transceiver is target for handset application. As always there is tradeoff between power consumption and operation speed. The higher reference clock frequency usually means better phase noise performance but more power consumption. This work tries to provide a flexible choice for the system designer to select between performance and power consumption for different system specification. The Wi-Fi alliance has defined 2.16GHz channel bandwidth for 60GHz band, Also all other standards in 2.4GHz and 5GHz band are using 20MHz, 40MHz, 80MHz or 160MHz bandwidth [4]. It is clear that, in order integrate the 60GHz capability to existing Wi-Fi system to form tri-band solution, the fractional-N mode is needed to reduce both system complexity and cost. At same time, 108MHz reference clock system is selected as integer-N mode to provide better phase noise and it is target for high data rate application by using more complex modulation method. The CMOS clock divider has 3 different working modes, namely low-power fractional mode, high performance fractional mode and integer mode. The total power consumption in the different working modes are 4mW, 9mW and 6mW respectively.

In this paper, both structure design and hardware implementation are discussed.

2. Dual Modulus Prescaler

The high speed prescaler is the most challenging part in the divider design because it operates at the highest input frequency. It is the bottleneck for programmable clock divider design. A dual-modulus prescaler (DMP) usually consists of a divide-by-2/3 or 3/4 followed by several divide-by-2 stages. Form the system specification, the divider range needed for the system is from 20 to 43 to cover the support reference frequency from 80MHz to 120MHz. There is no divide-by-2 in the DMP to fulfil the requirements coming from both divide modulus and speed. The 3/4 is better choice than 2/3 for this work.

Fig.1 shows the schematic of one type of 2/3 and 3/4 dual-modulus prescaler. Both of them has same hardware cost including 2 DFFs and one AOI logic gate. It is clear shows that the critical propagation delay path for both is same and that means the setup time requirement for the control signal “MC” is also equal. The “MC” is generated by modulus control block and that is clocked by “OUT” from the prescaler. Compare with them in this system, the available time to setup the divide modulus for 2/3 is 33% less than 3/4 at worst condition. Therefore 2/3 prescaler needs faster components than 3/4 prescaler, and more power consumption. At the same time, the internal net switch rate of the 2/3 prescaler is also more frequent than that in 3/4 prescaler, and that will cost more dynamic power in CMOS circuits. So the 3/4 dual modulus prescaler is better choice in both power consumption and system implementation without performance drop. The detailed discussion of the components for the proposed 3/4 dual-modulus prescaler is presented below. The AOI is implemented using normal CMOS structure and DFF is based on modified TSPC structure.

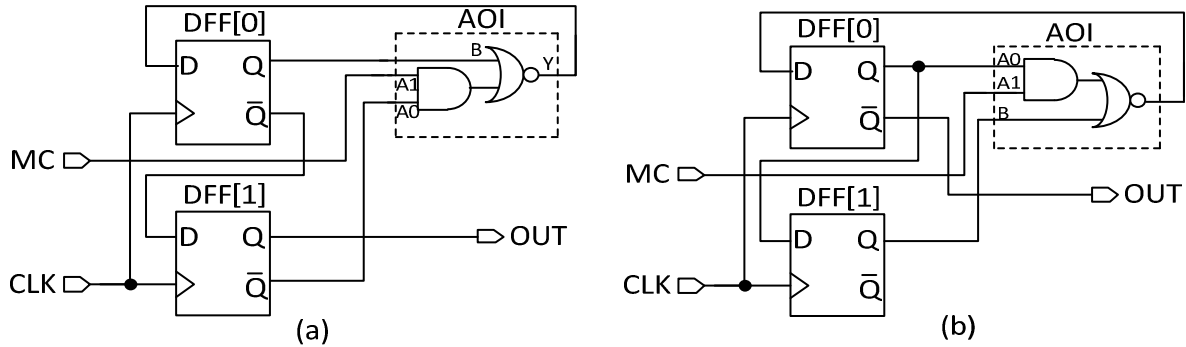


Figure 1 : (a) 2/3 dual-modulus prescaler , (b) 3/4 dual modulus prescaler

2.1 Modified TSPC DFFs

The TSPC DFF is widely used in high speed frequency divider and the E-TSPC DFF is proposed to further increase the operation speed of DFF. Fig2 shows the DFF's topology for a TSPC, an E-TSPC and the proposed DFF. The analysis of propagation delay for TSPC has deeply discussed as RC delay in [5]. The E-TSPC can achieve higher operation speed with same transistor size than original TSPC DFF due to lower load cap [6]. Compared with TSPC and E-TSPC topology in the Fig2, under the same working condition, it is clear that the E-TSPC will consume more power because of the short circuit current existing between VDD and VSS. For the proposed design, the modified TSPC DFF is used here to trade-off between speed and power as shows in Fig2(c). The first and third stage is same as TSPC and the second stage is based on the E-TSPC.

The transient simulation result for the first and second stage of the DFFs is show in Fig3. The simulation runs using 4GHz input clock. The result shows that TSPC structure cannot support to the required speed as the "S11" does not discharge to low, and both E-TSPC and the proposed DFF meet the speed requirement. The simulation result shows that the proposed DFF is just 20ps slower than E-TSPC DFF when "D" switches from high to low and almost has same response when "D" switch from low to high. While at the same time, the proposed design has much less power consumption than E-TSPC because of the short circuit period between VDD and VSS for first and third stage is removed by using CMOS structure.

The post layout simulation result shows the proposed DFF setup time is 30ps and clock to output delay is 110ps. The CMOS AOI's propagation delay is 120ps. That means that the proposed dual-modulus prescaler has no problem to work at 3.24GHz. The post layout simulation confirms that the circuit can work up to 3.5GHz at worst process corner and 100 degree temperature.

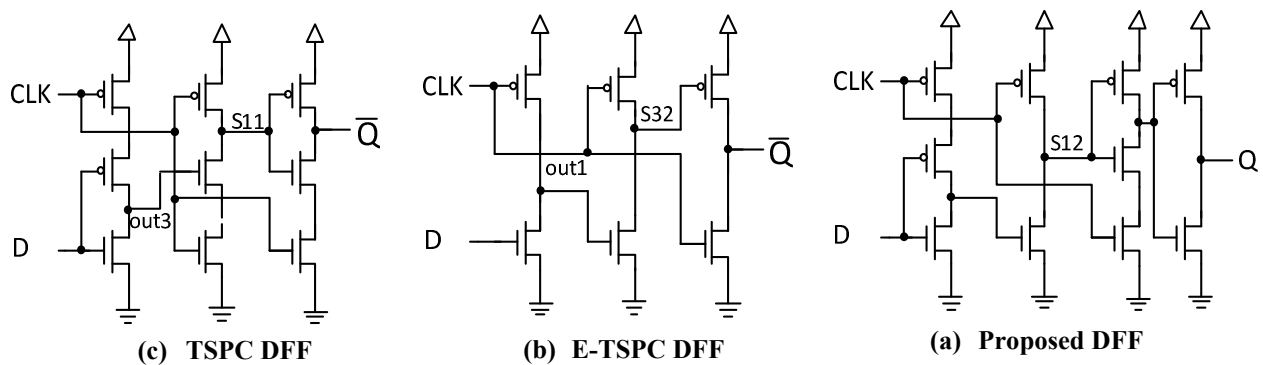


Figure 2 : DFF topology

3. 24-Modulus Divider Controller

The proposed wide multi modulus clock divider supports divider modulus from 20 to 43. This is used to cover the 60GHz frequency band with high resolution frequency step, and to support reference frequencies is from 80MHz to 120MHz. The divide rate definition need to support both Integer-N mode using 108MHz reference and the fractional-N mode using all other reference clock without external hardware cost. The block is implemented using standard 0.18 μ m CMOS logic gate from standard digital library to achieve best power consumption and small area.

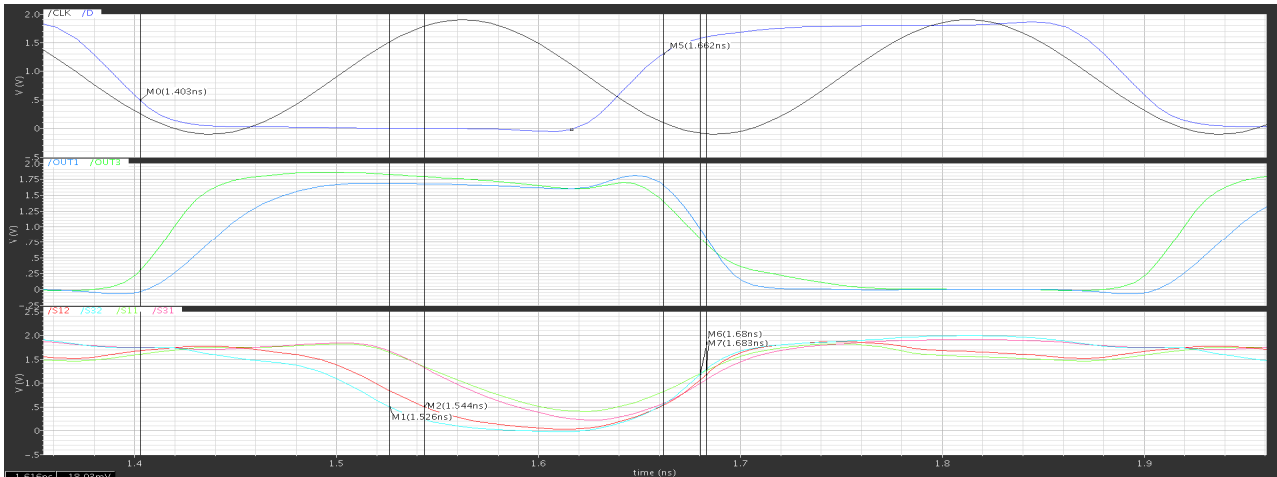


Figure 3 : Transient Simulation Result of DFF

The block needs to work at Giga Hertz range together with the 3/4 dual modulus prescaler mentioned above. As we know, It is a challenge for 0.18 μ m standard digital gate to work at Giga Hertz range. The operation speed must be carefully verified for the design. Fig4 shows the detail structure of the controller block. A 5 bits of control signal is used to specify the divide rate. The output signal “RefCLK” is also used as clock signal to update the divider rate. In the integer-N mode, control signal keeps constant all the time. While in the fractional-N mode, the control signal will change in time within some modes. The control sequence is generated by the MASH 1-1-1 module in this design.

There are 3 registers P, S and C implemented in the module. P and S is register to keep the corresponding control signal(S) or coded control signal (P). And C is 4-bits counter counting between 0 to P. The proposed module supports 24 working modulus and are separated into 2 groups, first group is from 20 to 31 and the other group is from 32 to 43. The corresponding control signal for the two groups are “00100” to “01111” and “10100” to “11111”.

The Control [4] is used to select between those two groups, and it is achieved by simply adding 12 more clock period when the signal is set to “1”. The implementation is done by adding 3 more divide-by-4 clock period to modify the programmable register “P”.

Control [3] is used to switch “P” between 5 and 7 (5+3 /7+3). The divider rate is from 20 to 23 and 24 to 31. Control [2:0] is used to set “S” which is used to control the time of MD reset and change the prescaler working mode. It is using conventional pulse-swallow structure. The proposed controller’s divide rate is $3 \times P + S - 1$, which is 1 clock period less than the normal structure using at least one clock period of divide-by-3 at all conditions. This helps to increase operation speed. From the Fig4, at the time when C equal to P, the MD is set to “1” and the prescaler works at divide-by-3. When the C count to (7-S), the MD will be resets back to “0” to let prescaler works at divide-by-4 mode. It is clear that the set and reset will not happen at same time in our design and it helps to reduce the complexity of the combination logic and increase the working speed.

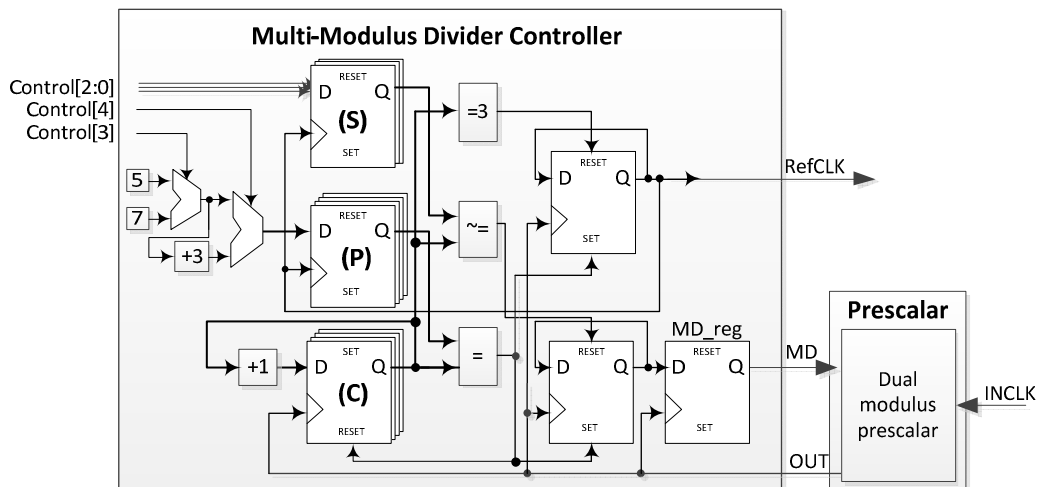


Figure 4 : Structure of Multi-Modulus Divider Controller

4. 3 Stage Delta Sigma Modulator

The MASH 1-1-1 structure is widely used to reduce the fractional spur in many fractional PLL [7]. It is used here to support the reference clock frequency of 40MHz, 80MHz and 120MHz compatible with existing Wi-Fi system to form the tri-band solution. The module will power off to save power in integer mode using 108MHz reference.

The 3 stages pipeline structure is used to implement the optimized MASH 1-1-1. The optimization between the accumulator length and performance trade-off is discussed in [8]. It can achieve 33% power reduction with a small performance drop. The ripple carry adder is used to implement the accumulator due to the simple structure and low power consumption. The module is also implemented using standard digital library. The maximum ripple carry adder chain is 10 bits for 120MHz system clock. The pipeline structure is optimized for the DSM modulator as shows in Fig5 below. The DSM structure makes full use of the existing internal registers in the accumulator and only 5 more registers are added (as shown in dark color).

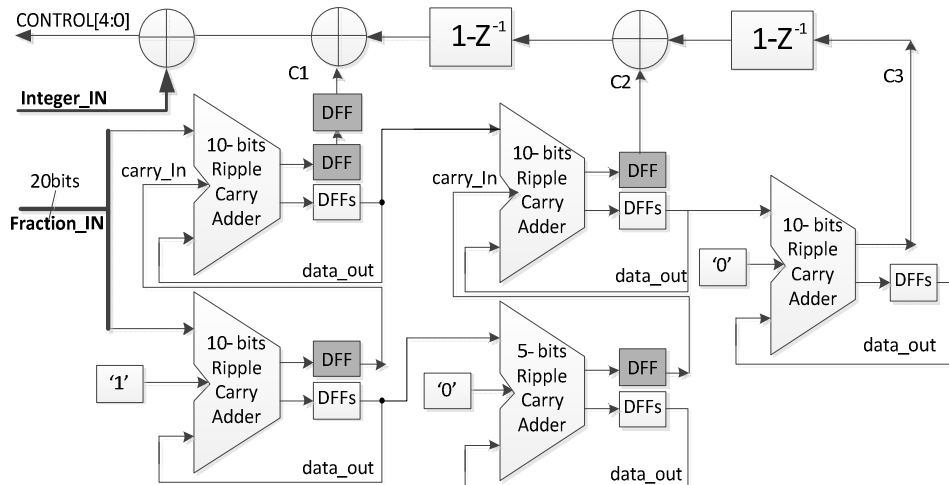


Figure 5 : MASH 1-1-1 DSM structure

5. Conclusion

The CMOS clock divider has 3 different working modes. First is low-power fractional mode, supporting reference clock from 27MHz to 40MHz by using one fixed divider-by-3 module. The total power consumption is 4mW including the prescaler. The Second mode is high performance fractional mode and the supported reference frequency for the mode is from 80MHz to 120MHz. The measured power consumption is 9mW. The last mode is integer mode, supporting reference clock of 108MHz for 802.11ad standard. The power consumption is 6mW.

6. References

1. IEEE Std 802.11ad-2012, 10.1109/IEEESTD.2012.639284.
2. China WPAN mmWave Liaison w/802.11, <https://mentor.ieee.org/11-11-134-00-00ad-china-wpan-mmwave-liaison-w-802-11>.
3. IEEE Std 802.15.3c-2009 (Amendment to IEEE Std 802.15.3-2003) , 10.1109/IEEESTD.2009.5284444
4. IEEE Std 802.11ac-2013, 10.1109/IEEESTD.2013.6687187
5. J.M RaBaey, A Chandrakasan, and B.Nikolic, Digital Integrated Circuits, A Design Prespective, Ser. Electron. and VLSI, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 2003.
6. J. Navarro Soares, Jr., and W,A . M.Van Noije, "A 1.6GHz Dual Modulus Prescaler Using the Extend True-Signal-Phase-Clock CMOS circuit Techique (E-TSPC)", IEEE JSSC ,Vol.34, NO.1, Jan 1999.
7. N.Fatahi, "Design of low noise fraction-N frequency synthesizer using sigma-delta modulation technique," Microelectronics proceedings (MIEL),2010, p369-372.
8. Y.Wang, K,Ma,"A delta-sigma fractional-N divider for a phase Lock Loop in 60GHz Transceiver" 10.1109/EDSSC.2011.6.117645 , p1-2.