

A 1.2-GHz bandwidth variable gain amplifier with continuous dB-linear control in 65nm CMOS

Zhengkao Lu, Kaixue Ma, and Kiat-Seng Yeo

School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798
luzh0001@ntu.edu.sg

Abstract

In this paper, a wideband variable gain amplifier (VGA) is designed in 65nm CMOS technology. The proposed VGA is composed of two cascading variable gain cells. Each gain cell employs a simple single-stage pseudo-exponential topology to realize continuous decibel in linear gain control and low power consumption. Two cascading cells realize a VGA with more than 50dB decibel in linear gain tuning range and 1.2-GHz -3dB bandwidth. The proposed wideband VGA consumes about 1.2mA current from a single 1.2V supply and is suitable for analog baseband signal processing in 60-GHz wireless communication systems. Furthermore, the proposed design is realized only based on CMOS devices without inductor and resistor which means small area and insensitive to process variation.

1. Introduction

In analog baseband circuits of various communication systems, variable gain amplifier (VGA) is always an essential building block that is used to increase the system dynamic range and implement the automatic gain control (AGC) function [1-8]. For Gbps wireless data links such as the 60-GHz millimeter-wave communication systems, wideband VGA design with low power consumption and decibel in linear gain control is necessary. The minimum -3dB bandwidth requirement for VGA in a 1-Gbps BPSK direct conversion receiver with a 0.5 roll-off-factor raised cosine pulse shaping filter is also around 1-GHz. Therefore, we present a wideband VGA topology design that meets the above-mentioned requirement. Multi-Gbps communications can be achieved by either increasing the circuit bandwidth or adopting more complicated modulation schemes such as QPSK and 16QAM.

2. Circuit Design and Analysis

To extend the gain control range, a VGA is usually required to possess decibel in linear gain control characteristic, which means a linear control voltage leads to an exponential output gain variation. There are numerous ways to realize such kind of decibel in linear gain control scheme, which can be categorized into three types: 1. Discrete gain control with digitally programmable gain steps based on current or resistor arrays, which is also called programmable gain amplifier (PGA) [2-3] [5-6]; 2. Continuous gain control with accurate dB-in-linear characteristic [1] [3]; 3. Continuous gain control with pseudo-exponential control function which means the dB-in-linear control is not so accurate and is limited to a certain range [7-8].

The continuous analog gain control mechanism is preferred in many situations not only due to its relative simplicity but also because in many situations such as the automatic gain control loop and OFDM-based applications, a continuous gain control without glitches is necessary. As mentioned previously, there are two major types of methodologies to realize the continuous dB-in-linear gain control. One method is based on the exponential I-V characteristic of the bipolar transistors or MOS transistors operating in exponential-lay region. This method, although leads to a wide range accurate dB-in-linear gain control characteristic, usually needs very complicated control circuitry to compensate various inaccuracies and temperature variation. The other method is based on designing the gain control function with a pseudo-exponential mathematical expression. This method usually has much simpler circuit topology while the dB-in-linear control range is dependent on how accurate the pseudo-exponential expression can be. In this paper, we follow the simplest pseudo-exponential expression realized by the circuit topology introduced in [8]. The major improvement of our proposed design is the compact design with folded-cascode topology to reduce the two-gain-stage structure in [8] to the one-gain-stage, which leads to lower power consumption and wider signal swing, making the proposed topology suitable for nano-scale CMOS technology realization with reduced supply voltage. Furthermore, the proposed design avoids using any resistor, making the circuit more compact and much less sensitive to process variation.

Figure 1 shows the proposed VGA cell circuit topology. M_1 through M_{10} composes the conventional folded-cascode amplifier topology that is more suitable for the low supply voltage in 65 nm CMOS technology. The biasing voltages V_{BP1} , V_{BP2} and V_{BN1} are generated by a conventional wide swing cascode current source. M_{R1} and M_{R2} are NMOS triode resistors that determine the gain of the amplifier. The two M_{R2} resistors are also implementing the common mode feedback function. The triode resistances are controlled by the gate control voltage V_C as shown in the figure. As the control voltage varies, the gain of the VGA also changes, which is given by:

$$Gain_{VGA} = \frac{2R_2}{R_1} \quad (1)$$

Where R_1 and R_2 are triode resistance of M_{R1} and M_{R2} that is mathematically given by:

$$R_1 = \left[k_n \left(\frac{W}{L} \right)_{MR1} (V_{DC} - V_{DC1} - V_{THN} + V_C) \right]^{-1} \quad (2)$$

$$R_2 = \left[k_n \left(\frac{W}{L} \right)_{MR2} (V_{DC} - V_{DC2} - V_{THN} - V_C) \right]^{-1} \quad (3)$$

Where V_{DC} is the DC level of the gain control voltage, V_C is the absolute amplitude of the gain control voltage and V_{DC1} and V_{DC2} are the DC biasing point as indicated in Fig. 1.

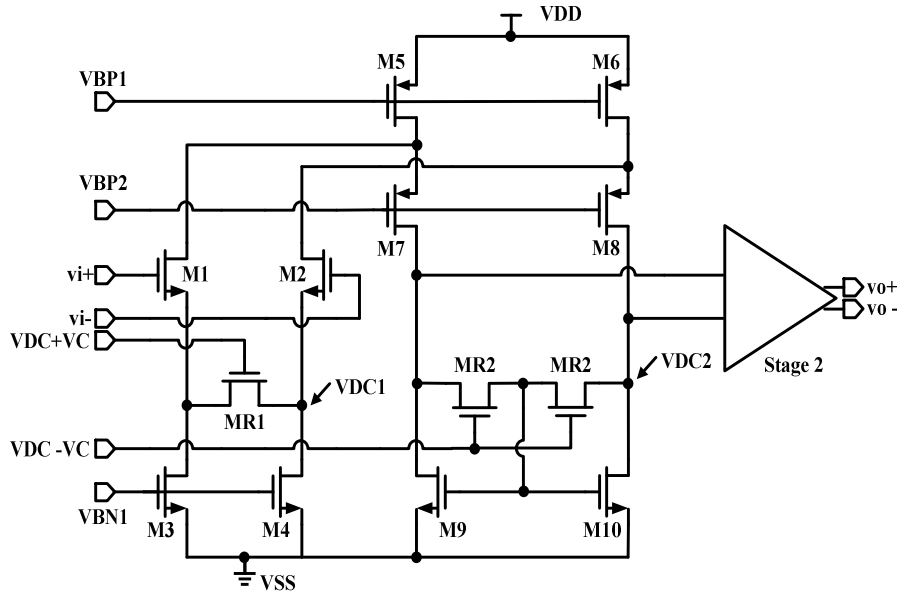


Fig. 1 Schematic of the proposed VGA

Substituting (2) and (3) into (1), we obtain:

$$Gain_{VGA} = \alpha \frac{1 + \frac{V_c}{\beta_1}}{1 - \frac{V_c}{\beta_2}} \approx \alpha \exp\left(\frac{\beta_1 \beta_2 - V_c}{\beta_1 + \beta_2}\right) \quad (4)$$

$$\alpha = 2 \left(\frac{W}{L} \right)_{MR1}^{-1} \left(\frac{W}{L} \right)_{MR2} \beta_1 \beta_2^{-1} \approx 2 \left(\frac{W}{L} \right)_{MR1} \left(\frac{W}{L} \right)_{MR2}^{-1} \quad (5)$$

$$\beta_1 = V_{DC} - V_{DC1} - V_{THN} \quad (6)$$

$$\beta_2 = V_{DC} - V_{DC2} - V_{THN} \quad (7)$$

According to (4), a linear control voltage V_C leads to an exponential voltage gain variation. However, this exponential relationship is based on mathematical approximation and the accuracy is less than 30dB. In this design, the typical value of V_{DC} is 1 V. The typical gain control voltage V_C tuning range in this design is -200mV to +200mV. The input and output common mode voltage are both designed to be 800 mV, which entails +/- 200 mV voltage swing and makes direct cascading of multiple VGA cells to achieve more gain control range possible. The second VGA stage shown in Figure 1 has the same topology and is realized using a PMOS input stage in a complementary way to shift the DC operating level, which is not shown in detail for simplicity.

3. Simulation Results and Discussion

The proposed VGA is composed of two cascading gain cells presented in Fig. 1. The circuit is designed and simulated in 60 nm CMOS technology and Cadence Spectre. Fig. 2 shows the simulated gain tuning range that exhibits a dB-in-linear control characteristic with more than 50-dB range (-30 dB to 20 dB). Fig. 3 shows the gain frequency response at maximum gain which is 20-dB with a -3 dB bandwidth of about 1.2-GHz. Fig. 4 shows the transient response of the VGA with +/- 100mV input and 6dB gain. According to Fig. 4, the proposed VGA shows good linearity with more than +/- 200mV output voltage swing. The simulated DC current consumption is about 1.2mA from a single 1.2V supply.

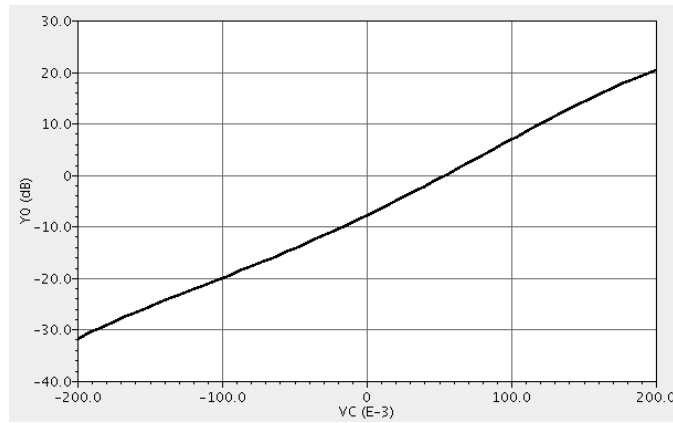


Fig. 2 Simulated gain tuning response of the proposed VGA

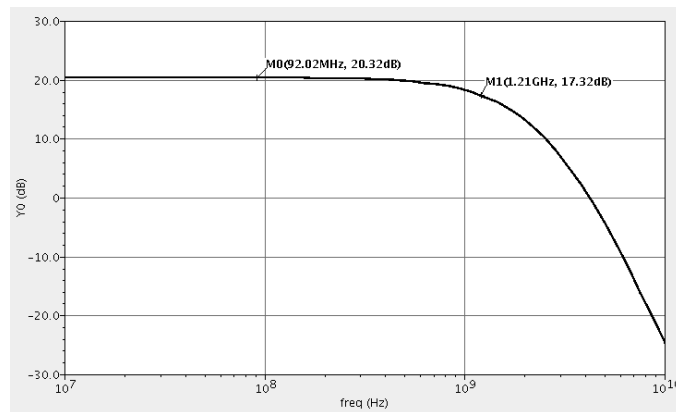


Fig. 3 Simulated gain frequency response of the proposed VGA at maximum gain

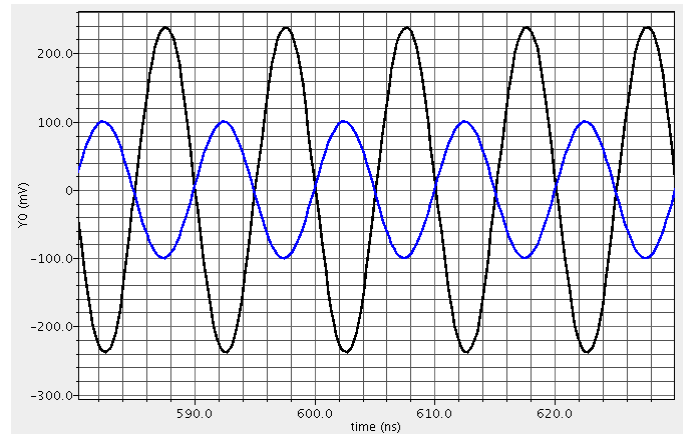


Fig. 3 Simulated transient response of the proposed VGA

4. Conclusion

A MOS transistor only VGA topology is presented in this paper. The proposed VGA adopts pseudo-exponential gain control to realize the decibel in linear gain tuning characteristic. The proposed VGA is designed and simulated in 65 nm CMOS technology. The simulation results shows the proposed VGA is suitable for 1-Gbps MMW communication systems such as the 60-GHz wireless data link.

6. References

1. W. Yanjie, B. Afshar, Y. Lu, V. C. Gaudet, and A. M. Niknejad, "Design of a Low Power, Inductorless Wideband Variable-Gain Amplifier for High-Speed Receiver Systems," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 59, pp. 696-707, 2012.
2. K. So-Young, R. Seung-Tak, and P. Chul-Soon, "A Precise Decibel-Linear Programmable Gain Amplifier Using a Constant Current-Density Function," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 60, pp. 2843-2850, 2012.
3. T. B. Kumar, M. Kaixue, and Y. Kiat Seng, "Temperature-Compensated dB-linear Digitally Controlled Variable Gain Amplifier With DC Offset Cancellation," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 61, pp. 2648-2661, 2013.
4. L. Chang, Y. Yue-Peng, G. Wang-Ling, X. Yong-Zhong, Z. Li-Jun, and M. Madhian, "A 5-Gb/s Automatic Gain Control Amplifier With Temperature Compensation," *Solid-State Circuits, IEEE Journal of*, vol. 47, pp. 1323-1333, 2012.
5. K. So Young, J. Jooyoung, O. Inn-Yeal, and P. Chul-Soon, "A 2.16 mW Low Power Digitally-Controlled Variable Gain Amplifier," *Microwave and Wireless Components Letters, IEEE*, vol. 20, pp. 172-174, 2010.
6. N. Huy-Hieu, N. Hoai-Nam, L. Jeong-Seon, and L. Sang-Gug, "A Binary-Weighted Switching and Reconfiguration-Based Programmable Gain Amplifier," *Circuits and Systems II Express Briefs, IEEE Transactions on*, vol. 56, pp. 699-703, 2009.
7. D. Quoc-Hoang, L. Quan, K. Chang-Wan, and L. Sang-Gug, "A 95-dB linear low-power variable gain amplifier," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 53, pp. 1648-1657, 2006.
8. I. H. Wang and L. Shen-Iuan, "A 0.18-um CMOS 1.25-Gbps Automatic-Gain-Control Amplifier," *Circuits and Systems II Express Briefs, IEEE Transactions on*, vol. 55, pp. 136-140, 2008.