6.2 GHz 0.5 mW two-dimensional oscillator array-based injection-locked frequency divider in 0.18 μm CMOS

Xiaopeng Yu, Xiong Song, Wei Meng Lim and Kiat-Seng Yeo

A new two-dimensional oscillator array-based injection-locked frequency divider is proposed. Instead of using the conventional analogue tuning technique or the one-dimensional delay chain, a two-dimensional array is implemented to digitally and precisely control the total delay in the oscillator core. This makes it possible to achieve a programmable delay, hence attaining potential programmable division ratios for the injection-locked divider. Fabricated in a standard 0.18 μm CMOS technology, a prototype chip, namely a divide-by-4/5 prescaler using this technique, is able to work up to 6.2 GHz with 0.5 mW power consumption from a 1.8 V supply voltage.

Introduction: The high-speed frequency divider is a key block in frequency synthesisers for wireless communications [1–4]. The dual-modulus or multi-modulus prescaler is the most challenging block among all kinds of frequency divider designs for its highest operating frequency in the system while variable division ratios are desired. The injection-locked frequency divider (ILFD), owing to its ultra-high operating frequency and low power consumption, has been regarded as an ideal candidate in high-speed frequency dividers. Several ILFDs with variable division ratios have been demonstrated in the recent literature [1–4]. However, the delay of the oscillator core in these dividers should be properly adjusted to obtain different division ratios, where proper sizing of devices or delay lines is needed. However, in today's very large scale integration (VLSI) systems, where implementation using a standard digital logic cell is highly desired, the self-oscillating frequency of the ring oscillator should be digitally and precisely adjustable. This Letter proposes a new two-dimensional ring oscillator array in an ILFD to achieve programmable division ratios.

Implementation of programmable delay in ILFD: The ILFD consists of an injector (e.g. a mixer) and a frequency selective block. The input signal is injected into the mixer and mixed with the divider's output signal, which produces a certain order of harmonic of the two signals. The frequency selective block filters out the undesired harmonics while keeping the desired frequency, which is equal to f_{in}/N. Hence, a divide-by-N operation is obtained.

The key component, the frequency selective block, can be a ring oscillator. Fig. 1 shows a simplified N-stage ring oscillator-based ILFD. Since the operating frequency of the ring oscillator is inversely proportional to the total delay of the loop, it is therefore possible to design an ILFD that is able to work at different operating frequencies by adjusting the delay in the oscillator core [3, 4]. In these designs, the delay in the oscillator core is obtained by switching of the delay cell or the proper sizing of transistors. In engineering applications, however, it is not easy to properly determine the self-resonant frequencies for different division ratios (or at different division ratios). For example, the delay chain in [3] is considerably long to achieve a wide programmable delay, hence accumulating potential variations in the self-oscillating frequency caused by process, temperature and supply voltage variations. As a result, a mismatch of the operating range exists between divide-by-N or $(N+1)$ operations. This suggests that the divide-by-N or $N+1$ is not able to work at the same input range. Better digital controlled delay lines are therefore very much desired to solve this issue.

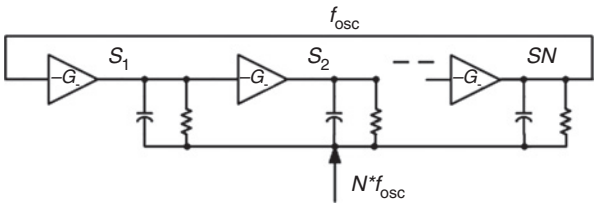

Fig. 1 *Conventional N-stage ring oscillator-based ILFD*

Fig. 2 shows a two-dimensional oscillator array first proposed in [5] as a multi-phase clock generator. It consists of several rows of ring oscillators, which is formed by several stages of dual-input inverters. As well as the delay stage at the horizontal direction, the dual-gate input inverters couple to each oscillator vertically. Hence, the overall plurality of the ring oscillators is not limited to one dimension any more. For example, the array oscillator includes first and second ring oscillators that are interconnected so as to form a closed-loop structure. In this ring oscillator array, the two rows of oscillators share a common oscillating frequency but of different phases. This characteristic makes the oscillator array suitable as multi-phase clock generator. In this design, where the dual-input inverting buffer stage is implemented, it is possible to manually adjust the total delay in this ring oscillator array. The buffer stage includes a first inverter having an input connected to the coupling input and a second CMOS inverter connected to the signal port.

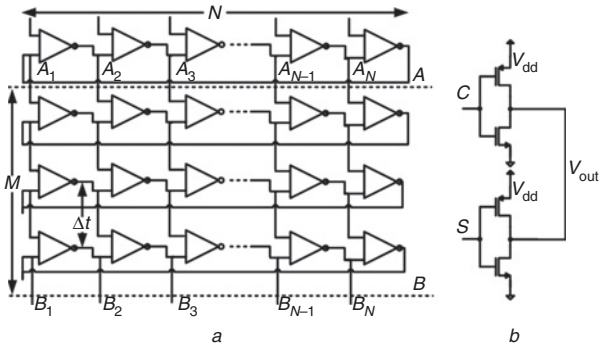

Fig. 2 *Two-dimensional oscillator array*

a Topology
b Dual-input inverter

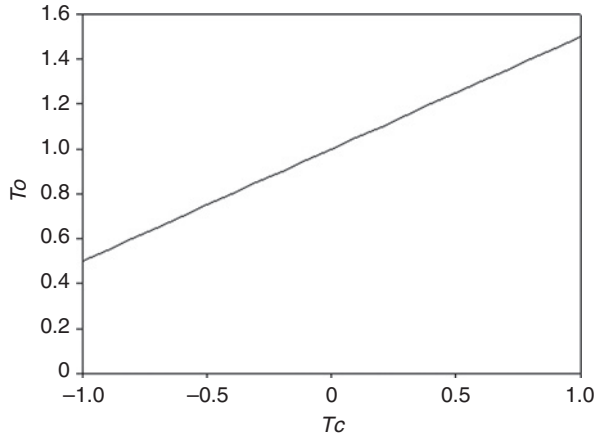

Fig. 3 *Total delay against stage delay*

In this two-dimensional array, the coupling input delay is now able to modulate the total buffer delay from the normalised total delay from $t_0 = 1$ to $t_0 = 1.5$. In a close array with a set of M ring oscillators, each having N buffer stages, for a reference clock sign of period T, the phase delay between successive nodes within a given array column, Δt can be expressed as

$$\frac{\Delta t}{T} = \frac{k + x2N}{2NM} \tag{1}$$

where x is an integer representing the number of extra oscillation periods spanned by the outputs of the corresponding buffer stages within each array column. From this relationship, we can achieve a programmable delay, hence a programmable self-oscillating frequency is achievable. Consequently, it can be used as a ILFD with programmable division ratios.

As shown in Fig. 3, the total delay To of the two-dimensional oscillator can be controlled by the stage delay Tc. Or by changing the total number of stages, the total delay that determines the self-oscillating frequency is programmable. For example, the first row of oscillators is the main one that provides the fundamental frequency. The second row of oscillators provides the modulation of the delay. The total delay of the ring oscillators is programmable for different division ratios by changing the total delay of the second oscillator.

Proposed dual-modulus prescaler: To verify this concept, a five-stage ring oscillator array is implemented, as shown in Fig. 4. It is configured as a divide-by-5 ILFD, while it is modulated as a divide-by-4 when the signal is injected from four sources in parallel. In this case when the *MD* signal is logically low (*MDB* is logically high), the total delay in this array is 10 units (stages). The modulus control signal connects a switch that can skip two stages at the second ring oscillator. In this case, two delay stages are switched off to save power consumption and the total delay becomes 8 units (stages). The self-resonating frequencies in these two cases become f_{osc} and $1.25f_{osc}$. The input frequency ranges for divide-by-4 and 5 are now perfectly matched. Even the absolute value of the self-oscillating frequency may change, thus the ratio remains. Similarly, different division ratios are possible by further extending the configuration of the delay stages. This design is suitable for present day digital CMOS VLSI technology, where the delay of the inverters can be precisely controlled.

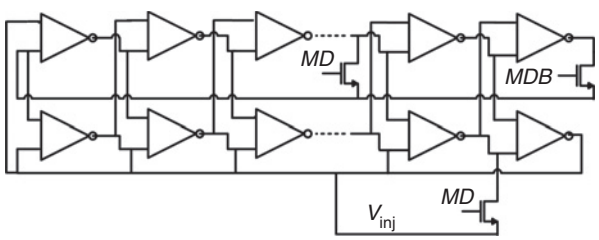

Fig. 4 *Proposed divide-by-4/5 prescaler*

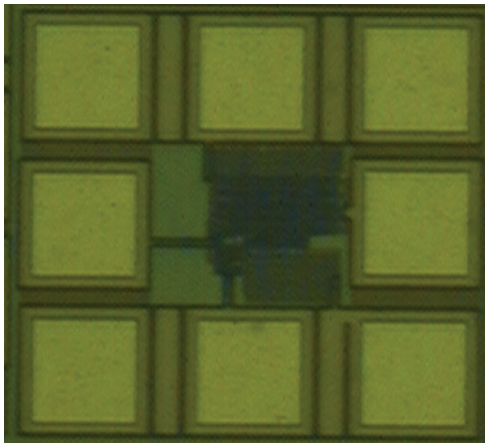

Fig. 5 *Die photo of proposed ILFD*

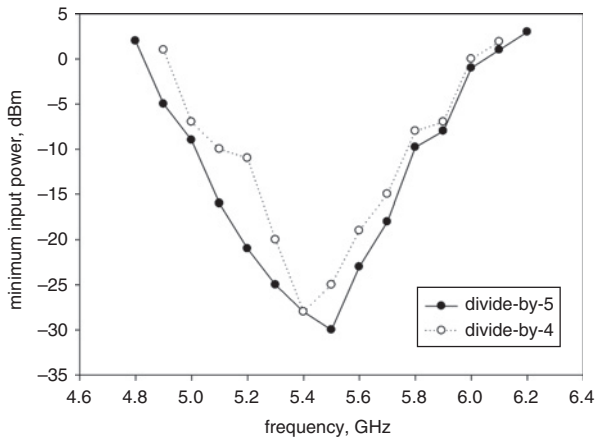

Fig. 6 *Measured locking range of proposed array-based ILFD*

The divide-by-4/5 ILFD was designed and fabricated using a standard 0.18 µm CMOS process. Fig. 5 shows the die photo of the proposed divider. The silicon area of the divider is about 40 × 70 µm, since the divider is MOS only. Including the test pads, the silicon area of the test chips is about 270 × 300 µm. Measurement was carried out on-wafer on the Cascade 12000 Probe Station. The input signal was from a signal generator, while the output was captured by an oscilloscope. The maximum operating frequency of the prescaler was measured at 6.2 GHz, whereas the minimum operating frequency was 4.8 GHz with an injected input power of 3 dBm. Instead of using a lower supply voltage as in [1, 2, 4], the standard supply voltage of 1.8 V for 0.18 µm CMOS technology was used since most of the circuits were digital blocks. The 4/5 dual-modulus prescaler dissipates 0.5 mW when operated at 6.2 GHz. Fig. 6 summarises the operating range of the proposed divide-by-4/5 prescaler. Unlike conventional designs that need proper sizing and adjusting of control voltage, the divide-by-4 and 5 operation matches well since the delay is fully-programmable in standard CMOS cells. Table 1 summarises the measurement results of these dual-modulus prescalers compared with the previously published work in terms of operating frequency range, division ratio and power consumption. This Table also demonstrates the trade-off among the functionality, power consumption and operation range. In the array-based ILFD, however, by using a redundant inverter stage, the operating oscillator is precisely programmable; hence the functionality is maximised by trading off power consumption.

Table 1: Comparison of measurement result with those in literature

Work	Process (µm CMOS)	Op. freq. (GHz)	Supply (V)	Power (mW)	Divide-by
[1]	0.18	5.6	1.2	0.22	4/5
[2]	0.09	0.85–0.9	1	0.03	$N/N+1$
[3]	0.13	5	1.2	0.35	2–6
[4]	0.18	6	1	0.22	4/5
This work	0.18	4.8–6.2	1.8	0.5	4/5

Conclusion: A low-power dual-modulus prescaler based on a two-dimensional ring oscillator is proposed. By using a two-dimensional array oscillator, the total delay of the oscillator core is hence programmable. The gap of the self-resonant oscillating frequencies for dual-modulus operation is well balanced. A prototype divide-by-4/5 prescaler was fabricated using a standard 0.18 µm CMOS process and has a measured operating frequency from 4.8 to 6.2 GHz, with a maximum power consumption of 0.5 mW.

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