Modified Inductive Peaking Direct Injection ILFD With Multi-Coupled Coils

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***Abstract*—In this letter, we present the design of a fully differential direct injection locked frequency divider (D-ILFD) in 65 nm CMOS process. Based on strong coupling of multi-coupled coils, we propose a modified inductive peaking in the D-ILFD to improve the locking range with a compact core area. The proposed injection locked frequency divide-by-2 divider demonstrates an operation frequency range of 6.7 GHz for a low injected power of -8 dBm and single-ended output power of -4 dBm. With a supply voltage of 1 V, the power consumption of the D-ILFD is 2.5 mW and the power efficiency (P_{out}/P_{DC}) is 8.3%.**

***Index Terms*—Direct injection locked frequency divider (D-ILFD), divide-by-2 divider, multi-coupled coils, strong coupling.**

I. Introduction

FREQUENCY divider is one of the integral parts of phase locked loop (PLL) frequency synthesizers. For millimeter-wave applications, the resonator-based direct- injection locked frequency divider (D-ILFD) is popular due to its inherent ability to achieve high operation frequency, high injection efficiency and low power consumption. However, the major drawback is its narrow locking range. Several techniques have been proposed to improve the locking range of the D-ILFD [1]–[7]. Simple varactor based tuning to increase the locking range is proposed in [1], [2]. However, the varactor tuning requires either additional external supply voltage or calibration circuitry when the D-ILFD is integrated in the PLL. Addition of resistors to lower the quality factor of D-ILFD tank is reported in [3]. Although the locking range is improved, the D-ILFD requires a high negative resistance to compensate for the increased tank losses and the output power of D-ILFD is low. Techniques to enhance the effective transconductance of injection transistor in D-ILFD are reported in [4], [5]. However, in [4] the area is large due to additional peaking inductors and the output power is low in [5].

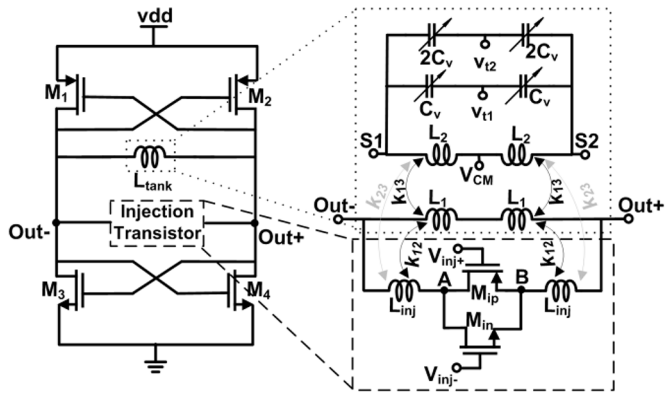

Fig. 1. Schematic of proposed D-ILFD divide-by-2.

In the D-ILFD, the signal injection is at the gate of the injection transistor and a higher signal injection can sometimes decrease the locking range [6]. For a given signal injection, the locking range of the conventional D- ILFD is given by [7]

$$LR \approx \frac{2\omega_o^2 L}{R_{eff}} \cdot \frac{|I_{inj}|}{|I_{osc}|} = \frac{2\omega_o^2 L}{R_{eff}} \cdot \frac{g_{m,inj}}{g_{m,cc}} \quad (1)$$

where L and R_{eff} are the overall inductance and effective parallel resistance of the ILFD tank respectively, I_{inj} is the injection current, I_{osc} is the ILFD core current,$g_{m,inj}$ and $g_{m,cc}$ are transconductance of the injection and cross-coupled transistor pair respectively. Therefore, from (1), the ILFD must have a large L (reduced capacitance) in the tank circuit to increase the locking range. Also, from (1), by increasing either I_{inj} or $g_{m,inj}$, a wider locking range can be achieved in the D-ILFD for a given signal injection.

In this letter, we propose a modified inductive peaking in the D-ILFD which employs multi-coupled coils with strong coupling. With the proposed inductive peaking technique, the effective transconductance of the injection transistor and the tank inductance is enhanced simultaneously. Also, the improvement in locking range of the proposed D-ILFD is achieved with no further increase in core area.

II. Circuit Design

The circuit schematic of the proposed D-ILFD is shown in Fig. 1. The cross-coupled transistors M_1–M_4 provide the required negative resistance to compensate for the tank losses and trigger the start-up of D-ILFD. The transistors M_{in} and M_{ip} in the D-ILFD are injection transistors ensuring direct connection of the differential outputs from previous stages. The core of the D-ILFD tank is formed by strongly coupled multi-coupled coils L_1, L_2 and L_{inj}, where L_1 is the primary tank inductor,

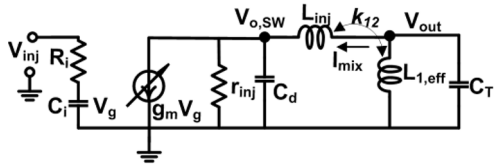

Fig. 2. Equivalent half of proposed D-ILFD injection transistor with modified inductive peaking.

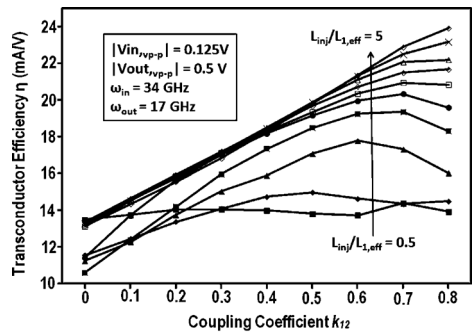

Fig. 3. Simulated transconductor efficiency with varying k_{12} and $L_{inj}/L_{1,eff}$.

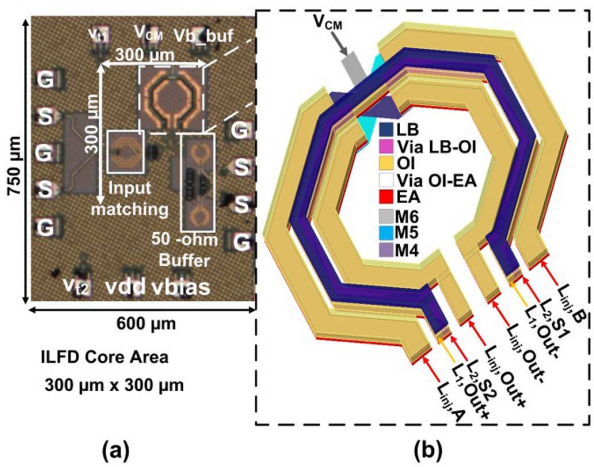

Fig. 4. Proposed D-ILFD (a) Die Microphotograph, (b) 3-D view of multicoupled coils (LB, OI and EA are the top 3metal layers in the foundry design kit).

L_{inj} is the peaking inductor magnetically coupled to L_1 and connected between injection transistor and D-ILFD output terminals. The secondary coil L_2 is stacked over the primary coil L_1 together with varactors C_{v1} and C_{v2} to discretely tune the center frequency of the D-ILFD by digital bits. With signal injection, the transistors $M_{in,p}$ in the proposed D-ILFD acts as a drain-pumped mixer [4], mixing the input signal ($\omega_{in} = 2\omega_{\text{out}}$) presented to the gate and the fundamental output (ω_{out}) at its drain. The half circuit model of the injection transistor is shown in Fig. 2. The mixing of the input signal ω_{in} with the output ω_{out} results in current I_{mix} injected into the LC tank given by

$$I_{mix}(t,\omega_{\text{out}}) = 2k_v g_{m,\max} \cdot v_{inj(t)} \cdot |V_{o,SW}(\omega_{\text{out}})| \cos(\omega_{\text{out}} t) \tag{2}$$

where, $g_{m,max}$ is the peak value of transconductance, $v_{inj(t)} = V_{in}\ cos(\omega_{in}t), k_v$ is the equivalent dc voltage, $V_{o,SW}$ is the output voltage at the drain/source terminal of $M_{in,p}$, and factor of 2 is due to differential output. Typically in the ILFD, increase in transconductance is achieved by increasing the (W/L) of $M_{in,p}$. However, this increases the

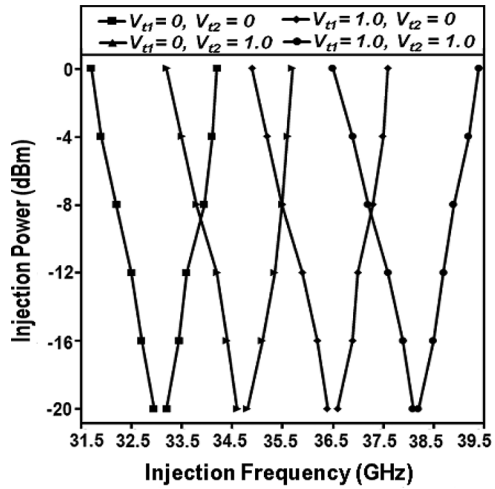

Fig. 5. Input sensitivity of D-ILFD.

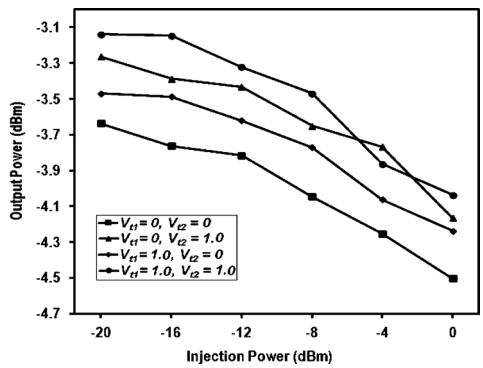

Fig. 6. Single-ended output power of D-ILFD.

capacitance across the LC tank and reduces the achievable locking range. In this work, a modified inductive peaking is proposed by coupling peaking inductor L_{inj} and tank inductor L_1 to increase $V_{o,SW}$. By incorporating a strong coupling between the peaking inductor L_{inj} and L_1, the voltage drop across $M_{in,p}$ is effectively boosted to improve I_{mix} and hence the locking range.

From Fig. 2, the voltage $V_{o,SW}$ at the drain and source of the injection transistor is given by

$$V_{o,SW} \approx V_{\text{out}} \cdot \frac{(L_{1,eff}+L_{inj}+M)+\omega_{\text{out}}^2(L_{inj}+M)(L_{1,eff}+M)C_T}{(L_{1,eff}+L_{inj}+M)-\omega_{\text{out}}^2(L_{inj}+M)(L_{1,eff}+M)C_T} \tag{3}$$

where V_{out} is the output voltage of the D-ILFD, $M = 2k_{12}(L_{inj}L_{1,eff})^{1/2}$ and C_T is the total capacitance. $L_{1,eff}$ in (3) is the equivalent transformed inductance due to inductor coils L_1, L_2 and varactors C_{v1} and C_{v2}

$$L_{1,eff} = L_1 + \frac{\omega_{out}^2 k_{13}^2 L_1 L_2 C_{v,T}}{1-\omega_{out}^2 L_2 C_{v,T}} \tag{4}$$

where $Cv,_T$ is overall capacitance of varactors C_{v1} and C_{v2}.

In the proposed D-ILFD, the proper choice of k_{12} and L_{inj} is important to maximize $V_{o,SW}$. However, due to the higher complexity of transistor large signal model, the current I_{mix} can be estimated by using simulations. The simulation result of the injection transistor with the proposed modified inductive peaking is shown in Fig. 3. The transistors M_{in} and M_{ip} are biased with a dc of 0.6 V with (W/L) of (40/0.065) μm and (60/0.065) μm

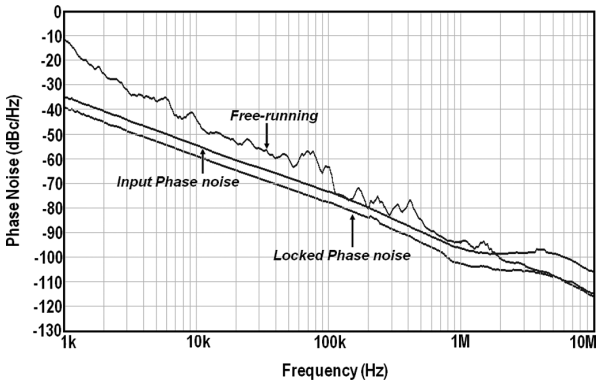

Fig. 7. Measured phase noise spectra.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF D-ILFD PERFORMANCE

Ref.	**This Work**	[3]	[2]	[5]	[1]
F_{center} (GHz)	**35**	28	23	26	36
LR (GHz) @					
Pin = -8 dBm	**1.8**	3.6	0.7	0.7	2.8
Pin = -5 dBm	**2.3**	5.0	1.2	1.3	-
Pin = 0 dBm	**2.9**	6.2	1.8	2.4	4.3
OR (GHz) @					
Pin = -8 dBm	**6.7**	3.6	4.3	0.7	6.2
Pin = -5 dBm	**7.1**	5.0	4.65	1.3	-
Pin = 0 dBm	**7.7**	6.2	5.4	2.4	6.5
P_{DC} (mW)	**2.5 /**	1.86 /	4.8 /	3 /	4.0 /
Core / buffer	**2.3**	2.64	3.8	2	-
Vdd (V)	**1.0**	1.2	1.8	1.0	0.8
P_{out} (dBm)	**-4.0**	-13.0	-2.8	-7.6	-3.0
P_{out}/P_{DC} (%)	**8.3**	1.11	4.25	3.48	-
FOM (%/mW^2)					
Pin = -8 dBm	**2.1**	0.2	0.83	0.18	-
Pin = -5 dBm	**1.1**	0.14	0.36	0.11	-
Pin = 0 dBm	**0.38**	0.05	0.17	0.07	-
Area (mm^2)	**0.3 × 0.3**$^{\#}$	0.5 × 0.56	0.22 × 0.27$^{\#}$	0.7 × 0.7	0.2 × 0.15$^{\#}$
Process Technology	**65nm CMOS**	0.13µm CMOS	CMOS in 0.18µm SiGe	0.18µm CMOS	65 nm CMOS

$$FOM = \left(\frac{(OR/F_{Center})}{P_{in}\cdot P_{DC}}\right)\left(\frac{P_{out}}{P_{DC}}in\%\right), \quad ^{\#} \text{ Core area,}$$

respectively. To simplify the results, the efficiency of $M_{in,p}$ defined as $\eta = |I_{mix}|/|V_{o,SW}|$ is plotted for varying k_{12} and $L_{inj}/L_{1,eff}$ ratio. From Fig. 3, it can be seen that, higher η can be achieved by increasing k_{12} and $L_{inj}/L_{1,eff}$ ratio. The results in Fig. 3 nonetheless, shows the trends for achieving an improved locking range using the proposed modified inductive peaking in the D-ILFD. In Fig. 3, η with $k_{12} = 0$ corresponds to the case with no inductive coupling between L_{inj} and $L_{1,eff}$. In the work, $L_{inj}/L_{1,eff}$ ratio is chosen to be 2.2 with $k_{12} = 0.6$. To further widen the operation range, the D-ILFD tank needs to have a wider frequency tuning range. In the proposed D-ILFD, L_2 is stacked over the primary coil L_1 to widen the frequency range using transformer based impedance transformation. The resulting variation in L_1 by discretely tuning the capacitance C_{V1} and C_{V2} connected to L_2 provides variation in D-ILFD center frequency eventually widening its frequency tuning range.

III. EXPERIMENTAL RESULTS

The proposed D-ILFD is implemented in Global Foundries 65 nm CMOS process and the die microphotograph is shown in Fig. 4(a). The D-ILFD occupies a core area of 300 μm $\times$ 300 μm including 170 μm $\times$ 180 μm for the multi-coupled coils implemented in the top three metal layers as shown in Fig. 4(b). The inductor coil L_1 is realized by combining the LB and OI metal layers. The peaking inductor L_{inj} is realized by combing the OI and EA metal layers with M5 and M4 metal layers for crossovers. The secondary inductor L_2 stacked to L_1 is realized in EA metal layer with M6 metal layer for center-tap connection. With a supply voltage of 1 V, the D-ILFD has a dc power consumption of 2.5 mW while the source follower buffer consumes 2.3 mW. The measured locked input frequency range as shown in Fig. 5 is 32.2 to 38.9 GHz for -8 dBm input power and 31.7 to 39.3 GHz for 0 dBm input power. The corresponding operational range (OR) is 6.7 GHz (18.8%) and 7.7 GHz (21.7%) for an input power of -8 dBm and 0 dBm respectively. The average single-ended output power of the D-ILFD across the locked frequency range is -4 dBm as shown in Fig. 6. At higher injected power levels, higher V_{GS} of $M_{in,p}$ reduce the quality of the D-ILFD tank and the output power [6]. The measured phase noise of the D-ILFD is shown in Fig. 7. The locked D-ILFD phase noise follows the input phase noise and the difference is close to theoretical value of 6 dB. In the far-away frequency offset, the locked phase noise of the D-ILFD follows the free running phase noise as shown in Fig. 7. The performance summary and comparison of the proposed D-ILFD is presented in Table I. Considering the locking range without discrete tuning in the secondary coils, the FOM for the proposed D-ILFD is 0.53 for an input power of -8 dBm.

IV. CONCLUSION

In this letter, a modified inductive peaking D-ILFD based on multi-coupled coils with strong coupling is presented. The presented inductive peaking technique increases the voltage across the injection transistors to increase its effective transconductance and the D-ILFD locking range with no further increase in chip area. Also, the operation range of D-ILFD is improved based on transformer based impedance transformation.

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