Transformer-Based Class-E CMOS Power Amplifiers

Alfred Lim[#], Kaixue Ma[*], *Senior Member, IEEE*, Kiat Seng Yeo [#&], *Senior Member, IEEE*

[#]School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore 639798
*University of Electronic Science and Technology of China (UESTC), China 610054
[&]Singapore University of Technology and Design (SUTD), Singapore 487372
Alfr0006@e.ntu.edu.sg, makaixue@uestc.edu.cn, kiatseng_yeo@sutd.edu.sg

Abstract

This paper proposes a transformer-based Class-E CMOS power amplifier (PA) for RF front-end. The PA is targeted to achieve a high power-added efficiency (PAE) and theoretical formulae are derived to demonstrate the PA design. A series inductor is magnetically coupled to the DC feed inductor such that the magnetic fluxes will be added. Thus, the sizes of both inductors are reduced significantly. The increased in the quality factor (Q_{ind}) of the on-chip inductors has resulted in a higher power-added efficiency of 50% at 2.4GHz.

Keywords: class-E, transformer-based and CMOS

I. INTRODUCTION

With the explosive growth of wireless and mobile communication systems, the demand for compact, low-cost and low power portable transceiver has increased dramatically. One of the technical issues in designing portable transceivers is the limited lifetime of the battery. The PA is typically the most power-hungry building block among the transceiver's building blocks. Therefore, the design of a high-efficiency radio frequency (RF) PA is the most important solution to overcoming the battery lifetime limitation in the portable communication system.

The Class-E PA as depicted in Fig. 1 has a maximum theoretical efficiency of 100%. It consists of a single output transistor that is driven as a switch and a passive load network. The passive load network is designed to minimize the drain voltage and current waveforms from overlapping [1], which causes the output power dissipation. The major difference between Class-E PA and others (e.g., classes A, B, AB, C, D and F) is that it incorporates the parasitic drain-source capacitance [2] to become part of the passive load network design, which is an advantage, especially in CMOS.

In Class-E PA, the circuit operation is determined by the transistor when it is on, and by the transient response of the load network when the transistor is off [2]. It greatly reduces the transistor power losses which occur during the off-to-on transition of the device, resulting in a high PAE. To minimize these power losses, the following conditions need to be met [1], [3]:

$$V_{DS}(t = t1) = 0 \quad (1)$$

$$\frac{dV_{DS}}{dt}\Big|_{t = t1} = 0 \quad (2)$$

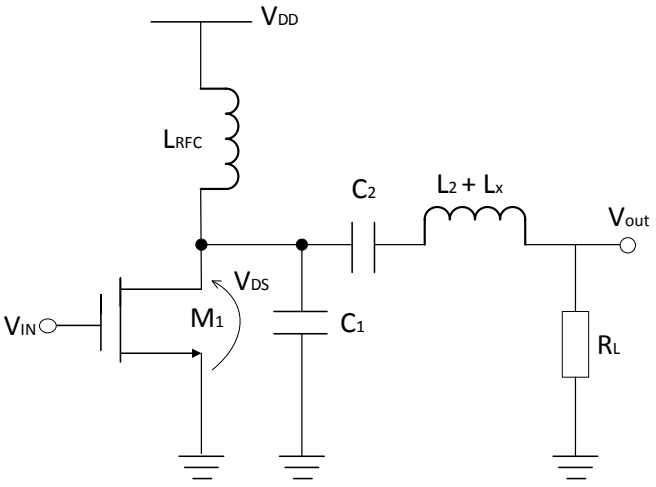

Fig. 1 Conventional Class-E PA with RF choke.

In the conventional Class-E PA, the RF choke (RFC) is assumed to have a sufficiently high reactance and the output current through the load resistor R_L is essentially a sinusoid at fundamental frequency. The tuned series tank circuit consists of C_2 and L_2. Under these conditions, the analytical design equations can be derived and are given by [4]:

$$R_L = 0.5768\frac{V_{DD}^2}{P_{out}} \quad (3)$$

$$C_1 = 0.1836\frac{1}{\omega R_L} \quad (4)$$

$$L_X = 1.1525\frac{R_L}{\omega} \quad (5)$$

Where $\omega = 2\pi f$, and f, V_{DD} and P_{out} are the operating frequency, supply voltage and the desired output power, respectively.

II. TRANSFORMER-BASED CLASS-E PA

The proposed PA with a finite DC-feed inductor is shown in Fig. 2. Using a finite DC-feed inductor instead of a large RF choke in the Class-E PA has several advantages [5] including:

- a reduction in the overall size and cost
- a higher load resistance for the same supply voltage and output power; yielding more efficient output matching networks

- large switch parallel capacitor C_1 for the same supply voltage, output power and load; enabling higher drain efficiency or higher frequency of operation
- a simplification in the design of the output matching network

The inductance constraint imposed by L_2 can be relaxed if the RF choke is replaced by the DC feed [2]. Therefore, to avoid the need for large inductance, different analysis methods have to be derived for optimization purposes.

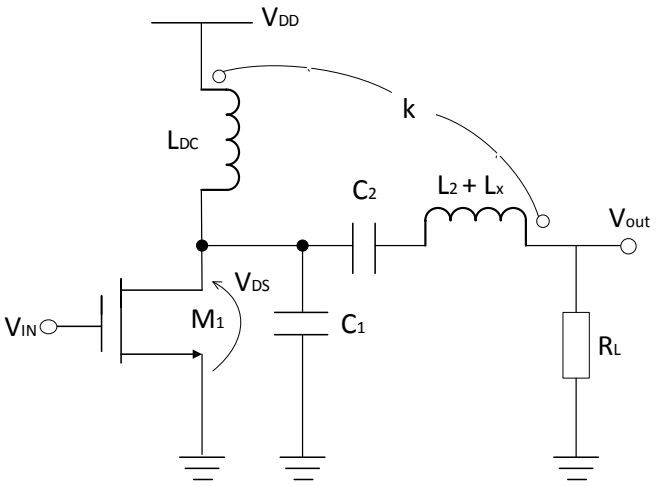

Fig. 2 Transformer-Based Class-E PA with finite DC-feed inductance.

When the transistor is off, the load network operates as a damped second-order system with initial conditions across C_1, C_2, L_2 and L_X. The time response depends on the Q of the network and appears as shown in Fig. 3 for under-damped, over-damped and critically-damped conditions. Using the Kirchhoff's loop law:

$$L_{eq}\frac{di}{dt} + R_L i + \frac{1}{C_{eq}}\int i\,dt = 0 \tag{5}$$

$$L_{eq}\frac{di}{dt} + R_L i + \frac{1}{C_{eq}}Q = 0 \tag{6}$$

$$L_{eq}\frac{d^2Q}{dt^2} + R_L\frac{dQ}{dt} + \frac{1}{C_{eq}}Q = 0 \tag{7}$$

This is a second-order linear homogeneous equation. Where $L_{eq} = L_2 + L_X$ and $C_{eq} = \frac{C1xC2}{C1+C2}$. With correct damping (i.e. $R_L^2 = 4L_{eq}/C_{eq}$), the voltage across C_1 can reach zero (i.e. $V_{DS}(t_1) = 0$) at the switch turn on. This will avoid the two undesirable conditions of under-damped and over-damped situations. The correct damping also gives zero slope to the switch (i.e. $\frac{dV_{DS}(t1)}{dt}|_{t=t1} = 0$) at the switch turn on. A nearly sinusoidal fundamental-frequency current flows in the output network.

To further reduce the size of inductors while keeping the same voltage across the DC feed and output series inductors, the two coupled inductors (DC feed and output series inductors) are inter-wound to form a transformer. This transformer-based configuration is introduced in the proposed Class-E PA topology. The amount of coupling between the two inductors is quantified by defining a mutual magnetic coupling denoted as *K*, which can take on any value between one and zero. Another way to describe the coupling between two inductors is with mutual inductance *M*.

$$K = \frac{M}{\sqrt{L_{DC}L_{eq}}} \tag{8}$$

Note that the dots in Fig. 2 are placed such that if current flows in the indicated direction, then fluxes will be added [6]. Thus, the inductance reinforces itself and, for a given inductance, the shape of both the DC-feed and output series inductors has a shorter length which gives a smaller series resistance. This exhibits a higher quality factor of the on-chip inductors. The higher quality factor also results in the higher power-added efficiency (PAE).

In addition, this design approach helps to minimize the chip area. Specifically, a larger inductance can be used without having an area overhead.

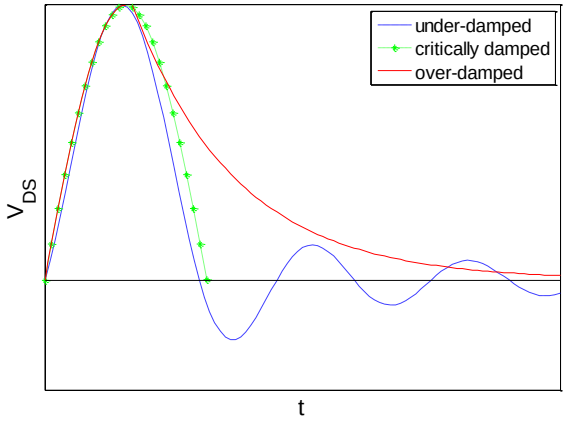

Fig.3 Class-E PA switch voltage.

III. SIMULATION RESULTS

In this section, the proposed design is used to compare with the uncoupled Class-E PA with finite DC-feed inductance in GLOBALFOUNDRIES' 65nm CMOS technology and is simulated in Cadence Spectre RF. A supply voltage of 1.2V and an operating frequency of 2.4 GHz are used.

An interleaved transformer is built by two inductors fabricated using the same metal layer whose coils (i.e. metal layers) are laterally interleaved. The interleaved topology provides full symmetry but has poor magnetic coupling. However, stacked transformers can also be used. They are made up of two identical inductors fabricated using different metal layers placed on top of each other. Stacked topology gives higher coupling factors, but inductors have different electrical parameters due to different metal layers.

The simulation results of PAE, power gain and output power versus input power at 2.4 GHz are shown in Fig. 4, Fig. 5 and Fig. 6 respectively. The proposed PA demonstrated an output power of 14 dBm, a peak power gain of 16 dB and a maximum PAE of 50.2%. While the uncoupled Class-E PA has an output

power of 12 dBm, a peak power gain of 15 dB and a maximum PAE of 43.8%.

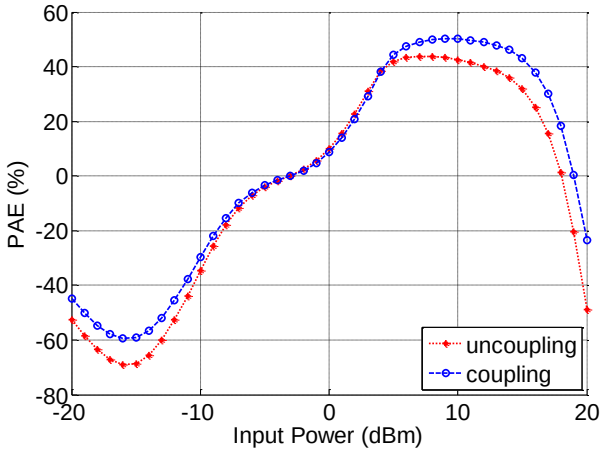

Fig.4 Simulated PAE versus input power at 2.4 GHz.

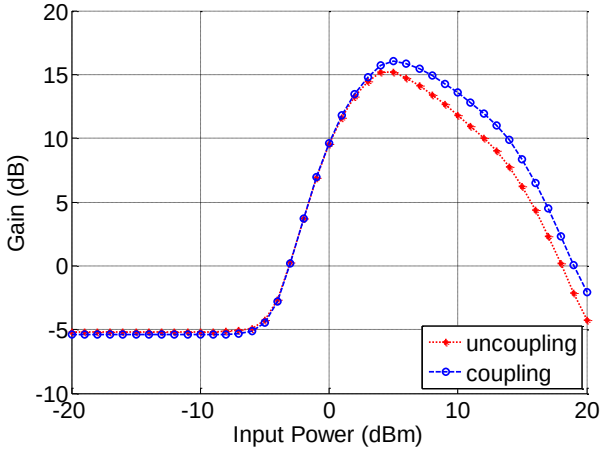

Fig.5 Simulated power gain versus input power at 2.4 GHz.

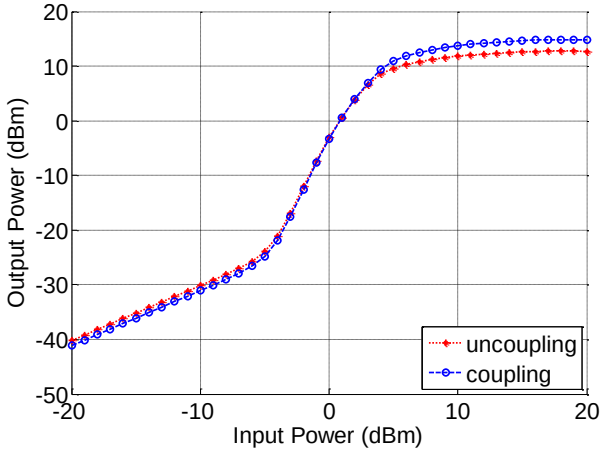

Fig.6 Simulated output power versus input power at 2.4 GHz.

IV. CONCLUSION

In this paper, a new Class-E PA using the transformer coupling effect to simultaneously reduce the chip area and improve the quality factor of the inductors is proposed. The design is simulated based on GLOBALFOUNDRIES' 65nm CMOS technology at 2.4 GHz. The comparison between the conventional design and the proposed Class-E PA with a finite DC-feed inductance shows an improvement of the output power, peak power gain and PAE by 16.7%, 6.7% and 14.6%, respectively.

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