A 32kb 9T SRAM with PVT-tracking Read Margin Enhancement for Ultra-low Voltage Operation

Anh-Tuan Do, Kiat-Seng Yeo and Tony Tae-Hyoung Kim
VIRTUS, School of Electrical and Electronic Engineering, Nanyang Technological University
Singapore 639798

***Abstract*— Diminishing bitline sensing margin at low voltage condition is one of the most challenging design obstacles for reliable SRAM implementation in nano-scale CMOS technologies. This paper presents a self-biased design technique that improves the bitline sensing margin during the read operation by sourcing a current which is the same as the total leakage along each bitline. It is able to automatically track changes in supply voltage, operating temperature and die-to-die process variations. Furthermore, a 9T SRAM cell is utilized to ensure that bitline leakage is data-independent. Simulation and measurement results using 65 nm CMOS process show that the proposed technique enlarge the bitline swing over a wide range operating temperature and operates successfully down to the supply voltage of 0.18 V.**

***Keywords*— SRAM, ultra-low voltage operation, read margin**

I. Introduction

Ultra-low power circuits are becoming increasingly popular in many green computing systems where sub-threshold or near-threshold operation is desirable with moderate performance [1]. However, operating circuits at ultra-low voltage leads to various challenging issues such as small noise margin, large device variations, etc. Unlike digital logic circuits which can be implemented with acceptable operation reliability, ultra-low voltage SRAMs face some extreme challenges due to their analog nature in various parameters such as cell stability, sensing margin, write margin, and bitline leakage current. Various circuit techniques have been presented to address the above challenges. One of the most significant changes made for ultra-low voltage SRAM design is the employment of decoupled SRAM cells with additional devices [2]. Decoupled SRAM cells improve cell stability by isolating the SRAM cell nodes from the read bitlines during read operation. Write margin has been improved by utilizing floating cell supply [3], boosted wordline voltage schemes [4], and negative bitlines [5]. Boosted wordline voltage schemes and negative bitlines augment the strength of write access devices while floating cell supply weakens the cross-coupled latches. Sense amplifier redundancy [6] has also been explored to tackle small sensing margin. Finally, leakage reduction techniques have been reported since leakage power is significant in ultra-low power SRAMs [7].

One of the main challenges that prevent SRAMs from operating at very low voltages is the diminished bitline voltage swing (i.e. the difference between reading “1” and “0”) caused by the reduced active current at low voltage and increased leakage current in nano-scale CMOS technologies. When total bitline leakage is comparable with or even larger than the actual read current, reliable sensing becomes insurmountable in conventional design. For example, at the supply voltage of 1V, the active read current is a few hundred thousand times larger than the bitline leakage current per cell but reduces to just a few hundred times at 0.3 or 0.4 V, as shown in Fig. 1(a). This makes a bitline structure with 256 cells per column work normal at higher supply voltage but fails to operate correctly at the supply voltage around 0.35 V.

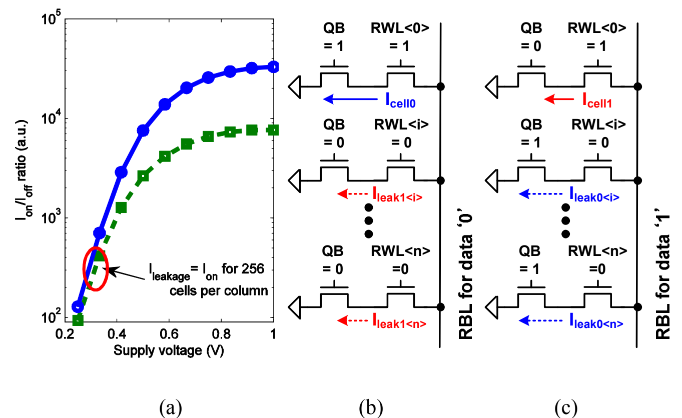


Fig. 1. (a) Ion/Ioff ratio of a conventional 8T SRAM design in 65 nm CMOS process at 80 ºC. (b)-(c) Schematic of a conventional 8T SRAM bitline structure in the worst case for reading data ‘0’ and ‘1’, respectively.

Fig. 1(b)-(c) illustrate a conventional decoupled 8T SRAM bitline structure where the 6T element is removed for the sake of simplicity. Read operation is enabled by activating a read wordline (RWL) and read bitlines (RBLs) are conditionally discharged in accordance with the accessed cell data. Ideally, RBL for read “1” (i.e. Q = 1 and QB = 0) remains at V_{DD} (i.e. I_{cell1} = 0) whereas RBL for read “0” is discharged to ground by I_{cell0}. The bitline sensing is conducted by differentiating the RBL discharging speed of data ‘0’ from that of data ‘1’. However, this structure has two undesirable effects at very low supply voltage condition: (1) both bitlines for reading “0” and “1” are discharged to ground with comparable speed, making it more difficult to sense; (2) each inactive cell along the bitline sinks data-dependent leakage, causing the worst case for reading “1” to happen when all inactive cells store “0” and the worst case for reading “0” happens when all inactive cells store “1”. As shown in Fig. 1(b), the leakage from a cell storing “0” is larger than that of a cell storing “1” due to its fully turned on bottom device (QB = 1). The total leakage in the worst case of reading “1” can be even larger than the sum of active current and total leakage in the worst case of reading “0”, causing the RBL for reading “1” to be discharged faster than that of RBL for reading “0”. Thus BL sensing can no longer work properly when the supply voltage scales from 0.4

978-1-4799-8391-9/15/$31.00 ©2015 IEEE

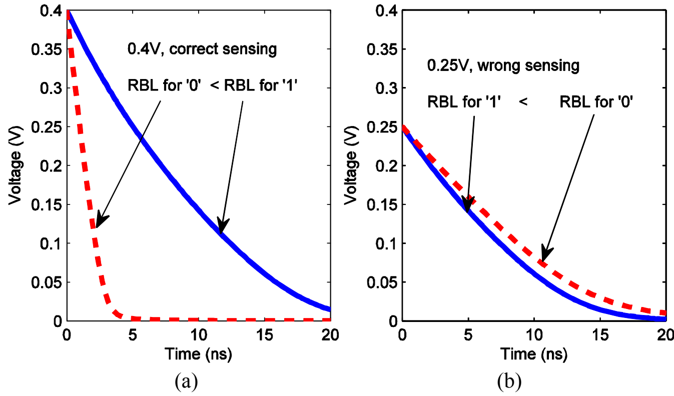


Fig. 2. Simulated RBL waveforms for illustrating read operation under extreme operating conditions (a) $V_{DD} = 0.4$ V. (b) $V_{DD} = 0.25$ V.

V to 0.25 V, as demonstrated in Fig. 2. Note that in Fig. 2(b), not only the two bitlines are almost indistinguishable; RBL for reading "1" is even smaller than that for reading "0", resulting in wrong sensing. Therefore, leakage-aware bitline structure design is highly required in low-voltage SRAM designs.

This paper aims at minimizing V_{DDmin} of the SRAM by tackling issues associated with the bitline leakage at extremely low supply voltage condition. We report a 9T SRAM that offers a constant bitline leakage, regardless of its stored data and a bitline biasing scheme that maximizes the bitline sensing margin at a wide range of operating temperature and supply voltages.

II. Proposed 9T SRAM Design

A. 9T SRAM cell for data-independent BL leakage

For the conventional 8T SRAMs, the worst case RBL of data '0' is determined by the pull-down current of 'I_{cell} + I_{leak_min}' while the worst case RBL of data '1' is the amount of the bitline leakage is governed by 'I_{leak_max}'. When 'I_{cell} + I_{leak_min}' is larger than 'I_{leak_max}', RBL can be correctly sensed. Otherwise, read failure occurs as explained in Fig. 2(b). To avoid this data-dependent bitline leakage issue, our 9T SRAM cell adds one more NMOS transistor to its read port. Fig. 3 illustrates the proposed SRAM cells storing data '1' and '0', respectively. If the cell stores data '0' (Fig. 3- left), the main bitline leakage path is through N_1 and N_2 since N_2 is fully turned on by the node QB while N_3 is off. In the case of storing data '0', N_3 is turned on while N_2 is turned off. Because the WL is also held at ground level, the main leakage path in this case is through N_1 and N_3 to ground. As a result, the new cell offers constant leakage, irrespective of its stored data. This principle is illustrated in Fig. 4. Since the amount of the bitline leakage is constant, it provides positive sensing margins regardless of the number of cells per bitline and the data pattern stored in a column. Fig. 5 demonstrates the simulated I_{read0}/I_{read1} ratio of the 8T and 9T bitlines. It can be seen that around 0.3 V, the total bitline current for reading '0' becomes smaller than that of reading '1' ($I_{read0}/I_{read1} < 1$) in the conventional 8T design while in the 9T design this ratio is always larger than 1, even at 0.2 V. Since the data-independent bitline leakage generates positive sensing margins, the bitline sensing will always give a correct outcome. Our proposed 9T SRAM has a similar leakage effect on the bitline compared to that in [8] but

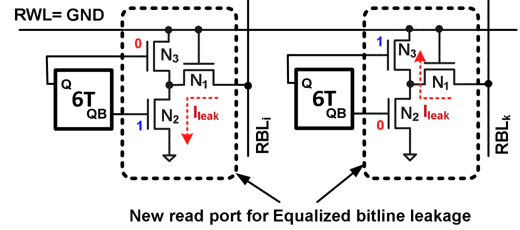


Fig. 3. New read port for data-independent bitline leakage.

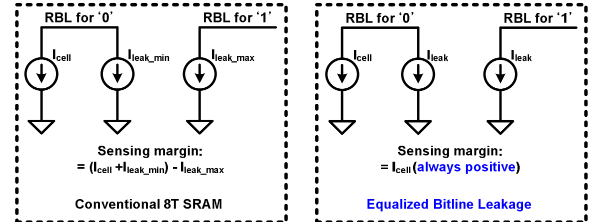


Fig. 4. Principle of the data-indepdent bitline leakage.

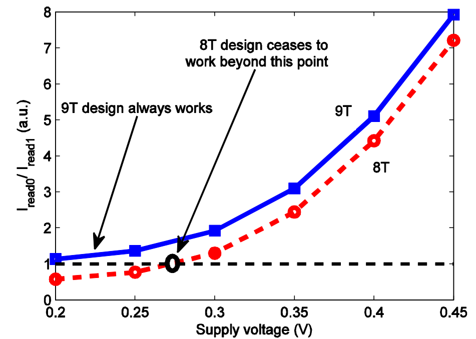


Fig. 5. Simulated Iread0/Iread1 ratio of the proposed 9T and the 8T cells.

we use that for decoupled single-ended cell. Furthermore, it does not affect the RBL parasitic capacitance and thus is more advantages when compared to that in [8].

B. Boosting current for maximizing RBL sensing margin

To implement reliable RBL sensing, it is desirable to improve both the RBL swing and the sensing window. In this work, we propose a novel bitline boosting current scheme to achieve this goal. Fig. 6(a) illustrates the proposed boosting current scheme employed in the proposed bitline. The basic read/write operation is the similar to the conventional 8T SRAM. The main difference is to eliminate precharge operation by turning off P_2 during standby. During read, a boosting current for RBL is provided by turning on P_2 while P_1 is constantly biased with an appropriate voltage. P_1 and P_2 form a RBL booster for each column. During read operation, the RBL boosters are activated, supplying pull-up boosting current to RBL. The RBL level for data '1' is formed at the level where the pull-up boosting current (I_{boost}) is balanced with the summation of the cell read current and the RBL leakage. This prevents RBL from being fully discharged down to GND by the pull-down leakage current, which expands the RBL sensing window. Compared to the conventional read operation where RBL is always pulled down to GND, forming a narrow RBL sensing window, the proposed scheme enables RBL to be sensed at any time after the RBL setup. Timing diagrams of the proposed and conventional scheme are shown in Fig. 6(b). This

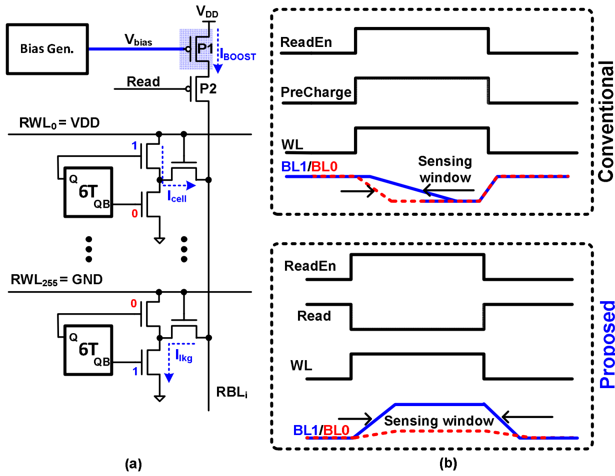


Fig. 6. (a) Schematic of the boosted bitline scheme [9] (b) timing diagram during a read operation of the conventional 8T and boosted bitline 8T.

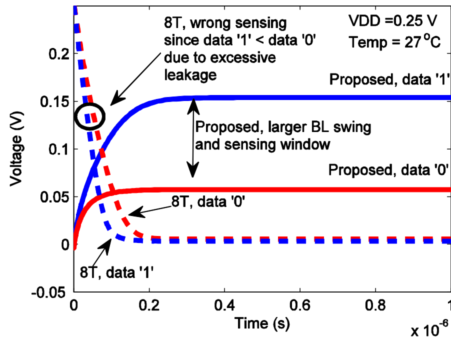


Fig. 7. Simulated proposed RBL waveforms and RBL swing of the conventional 8T at 27 °C. RBL levels of data '1' is higher than data '0' in the proposed design. However it is reversed in the 8T design, indcating a wrong sensing.

scheme is different from [10] whereby each individual BL leakage is measured separately. Although the scheme in [10] gives a more accurate compensation to each BL it significantly affects the performance as the leakage current must be measured each cycle. Furthermore, its area overhead is much larger. In our design, V_{bias} is applied to only the boosting PMOSs and there is no pre-charge operation. Thus, both area and performance efficiency are improved.

Fig. 7 compares simulated bitline waveforms of the proposed boosting and the conventional schemes. As expected, the proposed RBL boosting scheme shows a larger bitline swing and a wider sensing window. Furthermore, the 8T design leads to a wrong sensing since BL for data "1" is discharged even faster than that of data "0" at ultra-low voltage due to the data-dependent leakage.

C. PVT-tracking bias voltage generator

Even though the static RBL level improves the sensing window substantially, the RBL swing should also be large enough to be reliably sensed. To accomplish this, the strength of the RBL boosters needs to be carefully controlled. For example, if the RBL boosters are too strong, RBL for reading '0' will also be charged up to close to V_{DD}. On the other hand, if they are too weak, they will fail to raise the RBLs for data '1' up to required levels. The strength of the RBL boosters should be positioned so that it can maximize the bitline voltage

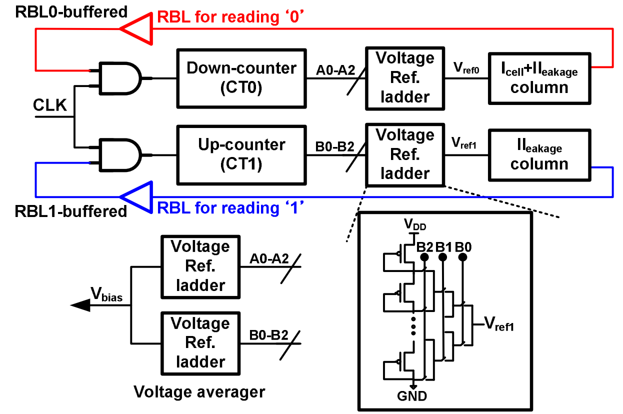


Fig. 8. Micrograph of the test chip fabricated in 65 nm CMOS process.

difference between the RBL of data '1' and that of data '0'. Different biasing voltage generates different RBL voltage levels and swings. Thus a PVT-tracking bias generator should be implemented to maximize the boosting effect

The generator must ensure that V_{bias} is hight enough so that I_{cell} can discharge RBL to ground while it is low enough to fight against the maximum leakage current. Fig. 8 shows the simplified schematic of our proposed bias generation scheme. It consists of two hard wired dummy columns, four voltage reference ladder and two counters. The first dummy column represents the read zero (i.e. $I_{RBL} = I_{cell} + I_{leakage}$) while the other represents the read one (i.e. $I_{RBL} = I_{leakage}$).

Initially, the down-counter (CT0) is at maximum, thus V_{ref0} is at V_{DD} and V_{RBL0} is at ground. As the CT0 counts, V_{ref0} steps down and I_{boost0} increases. This process continues until $V_{RBL0\text{-}buffered}$ tunrs high. This defines the minimum allowable value of V_{bias}. It also blocks the clock to CT0 and locks the output bits (A0-A2). Similarly, the bottom loop tracks the maximum allowable value of V_{bias} by using an Up-counter. The locked values of A0-A2 and B0-B2 are fed to two additional reference ladders to generate the final V_{bias} whose value is $(V_{ref0} + V_{ref1})/2$. Area overhead of this circuit is less than 5% (including the dummy columns).

III. CHIP IMPLEMENATION AND MEASUREMENT RESULTS

The proposed 9T design has been fabricated in a 65 nm CMOS process. Each bitline has 265 9T SRAM cells to test the robustness of the proposed idea. Micrograph of the test is shown in Fig. 9. Our measurement confirms that the proposed SRAM works properly down to 0.18V while the conventional 8T design with boosting fails to read "1" at 0.25 V. At 0.18 V, the proposed SRAM has a power consumption and access time of 1.2 µW and 4.1 µs, respectively.

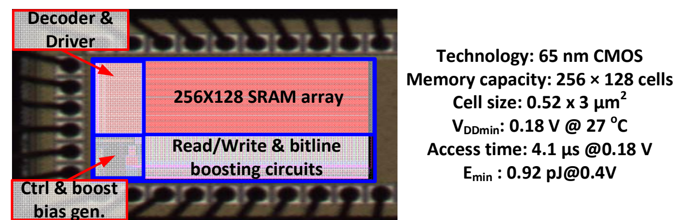


Fig. 9. Micrograph of the test chip fabricated in 65 nm CMOS process.

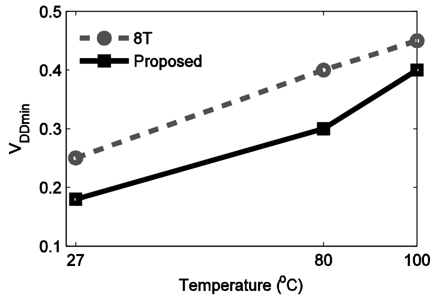


Fig. 10. Minimum supply votlage of the proposed and conventional SRAM at different operating temperature.

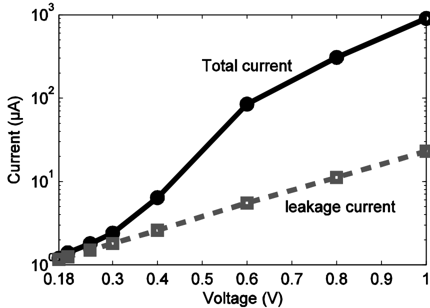
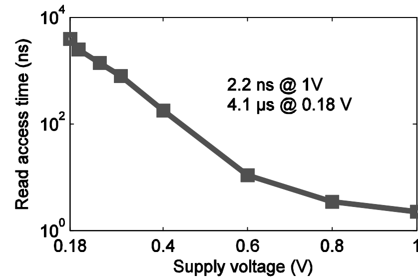


Fig. 11. Measured total and leakage current of the proposed design at room temperature.

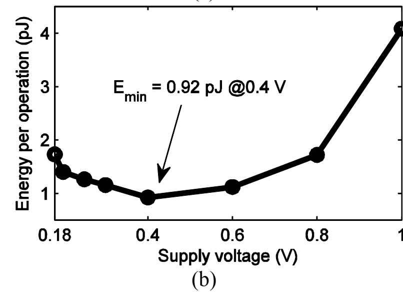
Fig. 10 compares the minimum operating voltages of the proposed and the 8T SRAMs with boosting at different temperatures. Although V_{DDmin} of both designs increases with temperature, V_{DDmin} of the 9T SRAM is always about 65 mV lower than that of the conventional one. As the supply voltage scales down, the proposed design offers much lower total current than when it operate at norminal supply voltage, as shown in Fig. 11. At extremely low supply (i.e. $V_{DD} < 0.4$ V), the leakage power becomes comparable to the dynamic power. Coupled with the fact that read access time increases exponentially in this region (Fig. 12(a)), total energy per access actually increases when supply voltage reduces to below 0.4 V. Consequently, the proposed SRAM achieves its minimum energy point of 0.92 pJ/access at 0.4 V, as shown in Fig. 12(b).

IV. CONCLUSION

A 32 kb 9T SRAM with data-independent leakage characteristic and column-based RBL swing boosting device has been implemented in 65 nm CMOS technology. It providing positive bitline sensing margins regardless of the number of cells per bitline. The boosted bitline read scheme offers an optimized bitline levels and bitline swings during a read operation. Furthermore, our PVT-tracking bias voltage generator ensures the correct sensing by tracking the maximum and minimum allowable biasing voltages of the case of reading ‘1’ and ‘0’, respectively. As a result, the proposed SRAM is able to operate down to 0.18 V at room temperature. The minimum operating energy is 0.92 pJ/read is obtained at 0.4 V in 65 nm CMOS process technology



(a)



(b)

Fig. 12 (a) Measued read access time and (b) minimum energy point of the proposed design at room temperature.

REFERENCES

[1] A. Wang and A. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," *Solid-State Circuits, IEEE Journal of,* vol. 40, pp. 310-319, 2005.

[2] T.-H. Kim, J. Liu, and C. H. Kim, "A Voltage Scalable 0.26 V, 64 kb 8T SRAM With V_{min} Lowering Techniques and Deep Sleep Mode," *Solid-State Circuits, IEEE Journal of,* vol. 44, pp. 1785-1795, 2009.

[3] M. Yamaoka, N. Maeda, Y. Shinozaki, Y. Shimazaki, K. Nii, S. Shimada, K. Yanagisawa, and T. Kawahara, "90-nm process-variation adaptive embedded SRAM modules with power-line-floating write technique," *Solid-State Circuits, IEEE Journal of,* vol. 41, pp. 705-711, 2006.

[4] B. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm Sub-threshold SRAM Design for Ultra-Low-Voltage Operation," *Solid-State Circuits, IEEE Journal of,* vol. 42, pp. 680-688, 2007.

[5] H. Pilo, I. Arsovski, K. Batson, G. Braceras, J. Gabric, R. Houle, S. Lamphier, F. Pavlik, A. Seferagic, C. Liang-Yu, K. Shang-Bin, and C. Radens, "A 64Mb SRAM in 32nm High-k metal-gate SOI technology with 0.7V operation enabled by stability, write-ability and read-ability enhancements," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, 2011, pp. 254-256.

[6] V. Naveen and A. P. Chandrakasan, "A 65nm 8T Sub-Vt SRAM Employing Sense-Amplifier Redundancy," in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, 2007, pp. 328-606.

[7] S. Cserveny, L. Sumanen, J. M. Masgonty, and C. Piguet, "Locally switched and limited source-body bias and other leakage reduction techniques for a low-power embedded SRAM," *Circuits and Systems II: Express Briefs, IEEE Transactions on,* vol. 52, pp. 636-640, 2005.

[8] A. Alvandpour, D. Somasekhar, R. Krishnamurthy, V. De, S. Borkar, and C. Svensson, "Bitline leakage equalization for sub-100nm caches," in *Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European*, 2003, pp. 401-404.

[9] A. T. So, T. Q. Nguyen, K. S. Yeo, and T. Kim, "Sensing Margin Enhancement Techniques for Ultra-Low-Voltage SRAMs Utilizing a Bitline-Boosting Current and Equalized Bitline Leakage," *Circuits and Systems II: Express Briefs, IEEE Transactions on,* vol. 59, pp. 868-872, 2012.

[10] K. Agawa, H. Hara, T. Takayanagi, and T. Kuroda, "A bitline leakage compensation scheme for low-voltage SRAMs," *Solid-State Circuits, IEEE Journal of,* vol. 36, pp. 726-734, 2001.