A Low Power Programmable Gain High PAE K-/Ka-Band Stacked Amplifier in 0.18 µm SiGe BiCMOS Technology

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***Abstract* — This paper presents a low power gain programmable high power efficient *K*-/*Ka*-band differential amplifier with current reuse topology. The amplifier achieves a best peak power added efficiency of 55.9% at the saturated power of +11.1 dBm and a variable gain from 1.8 dB to 16 dB with a 3-dB bandwidth from 21.8 GHz to 32.1 GHz. The design is fabricated in a commercial 0.18-µm SiGe BiCMOS process with maximum DC consumption of 12.5 mA from a single 1.8 V supply and a core amplifier design area of 500 µm × 450 µm.**

***Index Terms* — Current reuse topology, *K*-band, *Ka*-band, low power design, power added efficiency (PAE), programmable gain amplifier (PGA), SiGe BiCMOS, transformer coupled load.**

I. Introduction

The communication distance of the wireless communication system is mainly determined by the effective isotropic radiated power (EIRP) which is relied on the maximum transmitter drive power level and the antenna gain. This is attributed to the gain and linearity performance affected by the power amplifier which is also the most power hungry building block in the transceiver system. For low power design, it is desirable to achieve high output power with minimum dc power consumption and can be quantified using the power added efficiency (PAE) of the power amplifier.

A good linearity performance of the power amplifier design that delivers high output power (P_{sat}) can be achieved either by a marginal headroom constrained design using a large supply voltage [1]-[9] or by increasing the bias current [10].

To support the high data-rate applications as defined in the *K*-band (18 – 26.5 GHz) and *Ka*-band (26.5 – 40 GHz) standards, the transistor size has to be down-scaled resulting in a low breakdown voltage that limits the maximum supply voltage as well as the bias current density. To support the contradictory PAE requirement in power amplifiers with a high P_{sat}, various design techniques are realized such as the dual polarity supply voltage [1], multi-way low-loss parallel power combining [2], [4], [6], [7], adaptive biasing [3], switch-mode technique [5], and stacked amplifier stages [8].

The proposed design simultaneously achieves good linearity as well as improved PAE performance under the constraint of low power consumption by using a high quality-factor (*Q*) transformer coupled LC tank as load network and a stacked current reuse 2-stage differential amplifier topology with a controlled base current biasing. The proposed programmable gain amplifier (PGA) has dual-band switching capability that can operate at *K*- and *Ka*-band achieving a best peak PAE of 55.9%, a P_{sat} of +11.1 dBm, and a 4-bit gain control ranging from 1.8 dB to 16 dB.

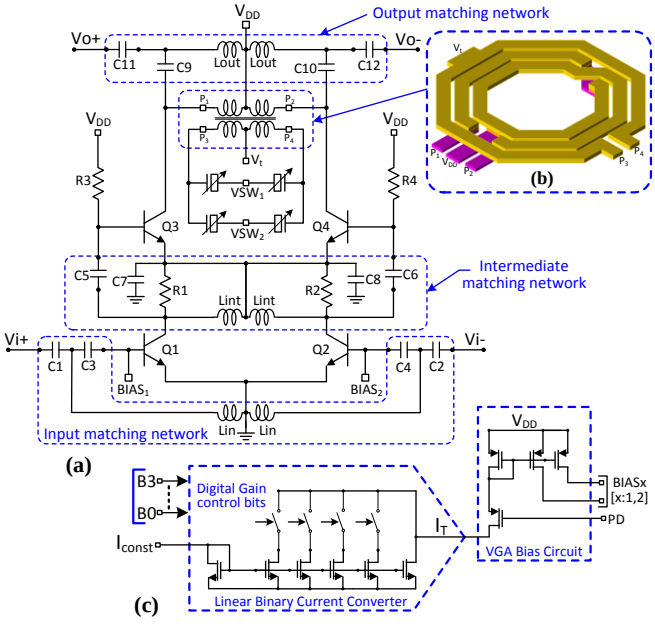

Fig. 1. Proposed *K*-/*Ka*-band PGA (a) circuit schematic (b) 3D view of 2-coil transformer (c) biasing circuit.

II. Circuit Design Description

The circuit schematic of the proposed dual-band PGA shown in Fig. 1 (a) is a 2-stage current reused fully differential broadband amplifier with a high *Q* transformer (Fig. 1 (b)) load that is magnetically coupled to a LC tank. The first stage (bottom) amplifier base current biasing is provided from a linear binary current converter as shown in Fig. 1 (c) while the top differential stage utilizes a fixed biasing. As the base

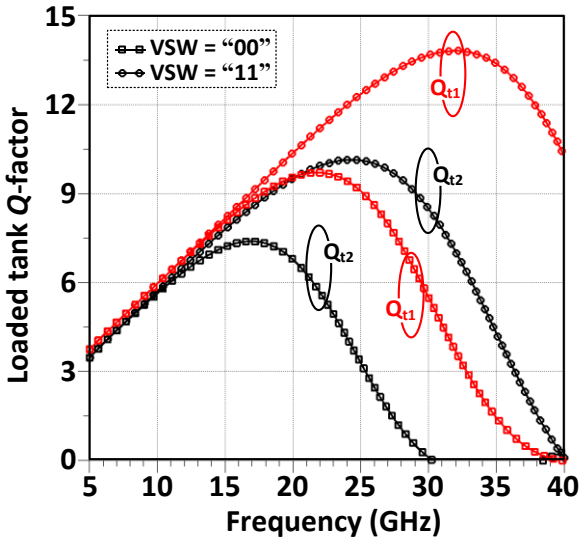

Fig. 2. Simulated single-end varactor bank loaded tank *Q* for two versions based on transformer size (d_t) and MOS varactor length (l_v) as Q_{t1} (d_t = 85 µm, l_v = 500 µm) and Q_{t2} (d_t = 94 µm, l_v = 650 µm).

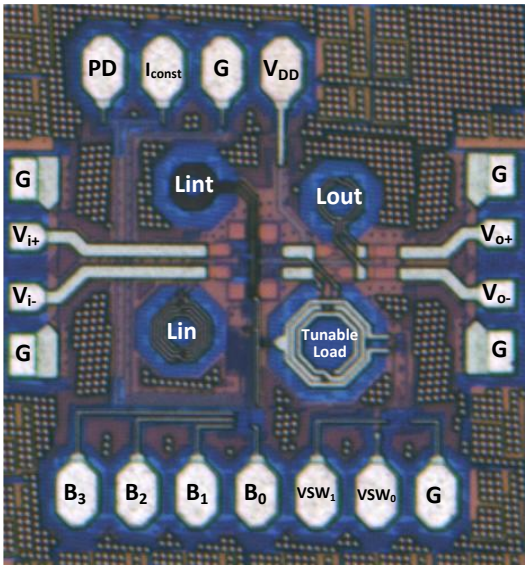

Fig. 3. Die Microphotograph of proposed *K*-/*Ka*-band PGA.

current of the first stage differential amplifier increases, the Q_1-Q_2 transistor pair moves from active to saturation region and results in the gain compression.

The LC tank loaded *Q*-factor is improved by reducing the MOS varactor-bank's channel length from 650 to 500 µm and simultaneously by decreasing the transformer's coil size from 94 to 85 µm. The simulation plot in Fig. 2 shows the *Q*-factor enhancement which are extracted from the EM simulation using Agilent Momentum EDA tool suite. This concurrently improves the PAE, the amplifier linearity and the peak gain performance, however at the expense of a narrowed frequency tuning range (VSW) constrained by the varactor's C_{max}/C_{min} ratio which are also evident from the on-wafer measurement results illustrated in the following Section III.

By increasing the range of the base bias current, the gain control range is increased as 1.8 dB to 16 dB. However, this increases the maximum dc power consumption to 22.5 mW.

III. Experimental Results

The proposed design is fabricated by using a 0.18 µm SiGe BiCMOS process from Tower Jazz Semiconductor and the die micrograph is shown in Fig. 3. The measured performance is obtained by using on-wafer probing with a differential 4-port GSSG RF probes and the dc probes set as 4-bit gain control (B_3~B_0), 2-bit band switching (VSW_1~VSW_0 = VSW), a constant current source (I_{const} = 50 µA), a power down control

TABLE I

Performance Summary of Wideband K-/Ka-band Drive Power Amplifiers

Ref.	Frequency [GHz]	Peak Gain [dB]	OP_{1dB} [dBm]	Peak P_{sat} [dBm]	Peak PAE [%]	P_{dc} [mW]	V_{DD} [V]	Die area [mm²]	Technique / Topology	Technology
[1]	24	19	15.7	19	24.7	-	± 3.6	0.56 × 0.67	reverse body bias	0.18-µm CMOS
[2]	16.5 to 28	37.6	15*	19.4	22.3	228	2.4	2 × 1	driver + 2 parallel PA	0.18-µm SiGe
[3]	20 to 25	11.9	15.4	17.4	12	108	3.6	0.83 × 0.48	adaptive bias	0.18-µm CMOS
[4]	24	8	20	22	20	504	3.6	0.6 × 0.7	4-way combining PA	0.18-µm CMOS
[5]	24 to 31	10.3	15	17.1	40.7	-	2.2	0.6 × 0.45	1-stage class F^{-1}/F	0.13-µm SiGe
[6]	31.9 ± 2.4	46.8	15.4	19.4	6.18	1410	2.5/1.4	3.5 × 4	4-way combining MSL¥	0.12-µm SiGe
[7]	17 to 35	12	21~22	22.5~23.5	30~40	498	4	1.5 × 1	binary combining PA	0.15-µm pHEMT
[8]	37	5.2	14.5/17.5	20.2/21.4	11.2/7	-	3.6/4.4	0.28	2 stacked cascode	45nm SOI CMOS
[9]	18 to 33	15.2	16	19.5	10.2	711	3.6	1.41 × 0.61	darlington + TLT£	0.18-µm CMOS
[10]	27 ± 1.5*	14.5	-	14	13.2	169.2	1.8	0.7 × 1.2	substrate-shield MSL¥	0.18-µm CMOS
This work	**21.5 to 29.9** **21.8 to 32.1**	**1.7 to 16.3** **1.8 to 16**	**8.3** **9.6**	**9.2** **11.1**	**35.3** **55.9**	**22.5**	**1.8**	**0.89 × 0.81**	**stacked amplifier + tunable load**	**0.18 µm SiGe**

£transmission line transformer, ¥micro-strip line, *estimated value from the measurement plot

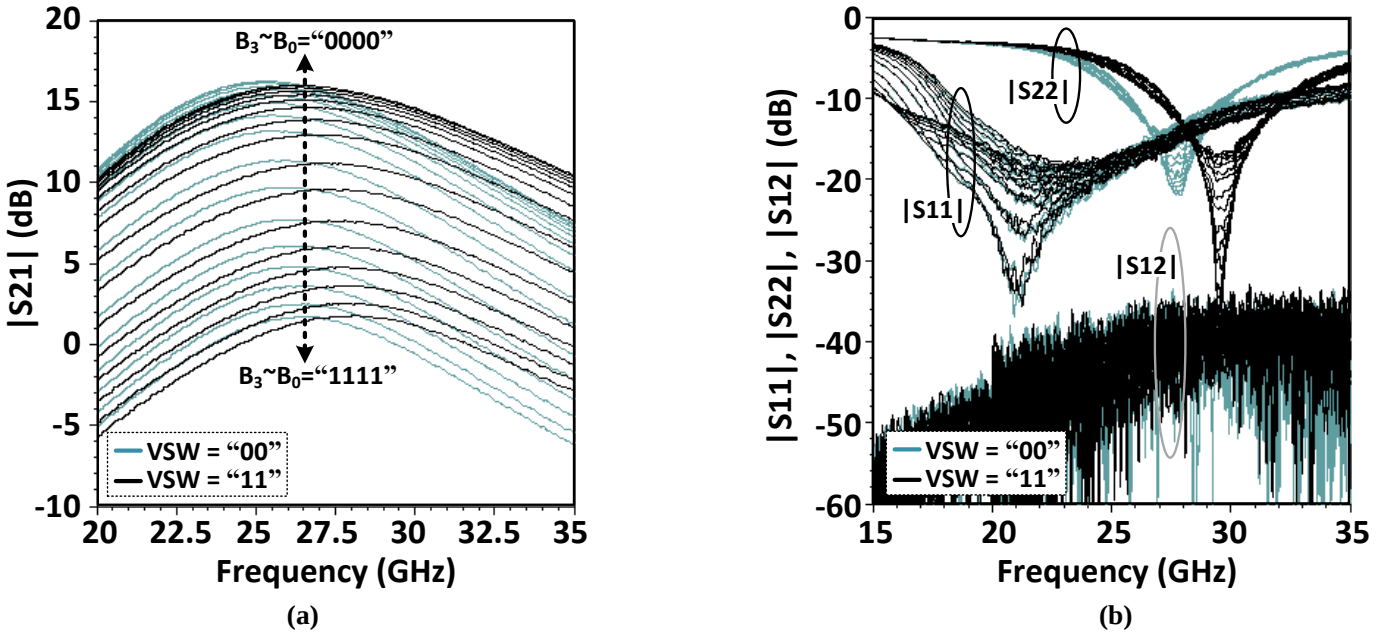

Fig. 4. Measured *S*-parameter variation based on B_3~B_0 (16 steps), band switch based on VSW (2 steps) (a) gain (b) return loss and isolation.

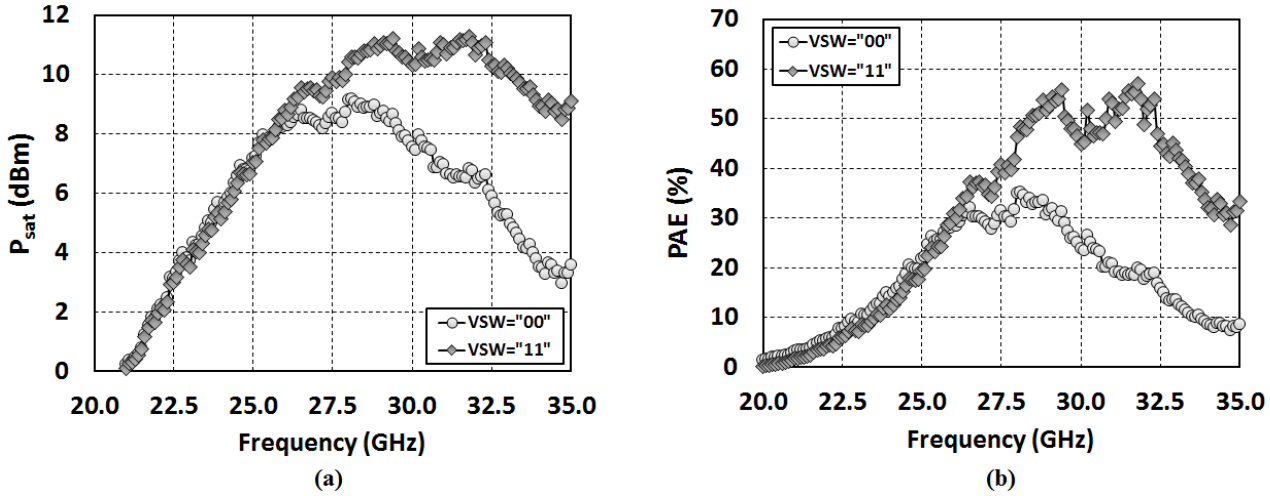

Fig. 5. Measured linearity performance over the two bands (VSW) of proposed design with maximum gain (B_3~B_0= "0000") (a) P_{sat} (b) PAE.

(PD) and dc supply voltage (V_{DD} = 1.8 V). The voltage levels for digital control bits (B_3~B_0, VSW and PD) are 0 and 1.8 V.

The measured *S*-parameters are obtained for the 16-gain steps using B_3~B_0 and for the two bands (VSW) as shown in Fig. 4. The proposed design achieves a variable gain from 1.7 to 16.3 dB over a 3-dB bandwidth from 21.5 to 29.9 GHz for band #1 (VSW = "00") and a gain variation from 1.8 to 16 dB over a 3-dB bandwidth from 21.8 to 32.1 GHz for band #2 (VSW = "11"). The input return loss is improved by using a center tap differential inductor (L_{in}) of 0.22 nH and a *Q* of 12.7 at 30 GHz frequency.

The measured P_{sat} and peak PAE plots are obtained for both the frequency bands at the maximum gain condition as shown in Fig. 5. The large signal 3-dB power bandwidth measured from the P_{sat} plot in Fig. 5 (a) for the low band (VSW = "00") is 24.3 to 32.4 GHz and for the high band (VSW = "11") is from 25.8 to 35 GHz. Based on the plot in Fig. 5 (b), a high PAE in addition to a better linearity performance is achieved by selecting VSW = "11".

The dc leakage current during power down mode is 102 µA obtained by setting PD = 1.8 V.

Table I summarizes the measured performance of proposed PGA design and compares it with the state-of-the-art works. The measured results shows a simultaneous improvement of the amplifier gain, the highest PAE, and the lowest power consumption from a 1.8 V supply voltage which are desirable for mobile wireless applications.

IV. Conclusion

A four bit gain programmable high power efficient *K*-/*Ka*-band differential amplifier with current reuse topology is proposed and implemented in this work. By using a stacked architecture and a high *Q* transformer coupled load, the proposed design achieves a best peak PAE of 55.9% and a P_{sat} of +11.1 dBm measured at 29.5 GHz frequency. This performance enables this design to be a suitable candidate for integrating in low power SoC designs.

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