High-Frequency Noise Modeling of MOSFETs for Ultra Low-Voltage RF Applications
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Abstract—In this paper, analytical models for high-frequency drain-current noise, gate-current noise, and their cross-correlation of MOSFETs are presented with an emphasis on the weak- and moderate-inversion regions. Unified expressions offering excellent continuity and smoothness from weak- to moderate- and strong-inversion regimes were developed. It is demonstrated that the continuity and the accuracy of the calculated four noise parameters, such as minimum noise figure, normalized noise resistance, and optimum source conductance and susceptance, are significantly improved in the weak- and moderate-inversion regions by using the proposed unified noise model, which includes the junction-induced drain-current noise. A figure-of-merit is introduced to determine the optimum gate biasing point of MOSFETs, where high gain can be achieved at low driving power and low operating noise. The results obtained from the proposed model manifest good agreement with the on-wafer measurement results.

Index Terms—Channel thermal noise, high-frequency (HF) noise, induced gate noise, moderate inversion, MOSFET, noise parameters, subthreshold, thermal noise, weak inversion.

I. INTRODUCTION

CMOS has advantages of offering very low-power consumption and achieving extremely high unity-gain frequency due to the continued down-scaling of technology. The demand for ultra low power is getting higher, directing to the exploitation of ultra low-voltage and subthreshold design for RF application [1], [2]. Accurate models predicting the high-frequency (HF) noise characteristics in the low inversion region is essential for the application in subthreshold RF integrated circuit (RFIC) design. However, the HF noise has been studied mostly in the strong-inversion region [3]–[11]. These models cannot ensure good accuracy and continuity of current noise power spectral density in moderate- and weak-inversion regimes. The existing models for all regions of operation such as [12] underestimated the noise level in the subthreshold region at HF, as reported by [13]–[16]. At HF, induced-gate noise is generated in MOSFETs and becomes more prominent under subthreshold condition. The induced gate noise model and its cross-correlation with channel thermal noise for the strong-inversion region has been derived by [17]. Although [18] derived the subthreshold model for induced gate noise, the study lack of experimental verification for the subthreshold region.

The authors have presented a unified HF drain-current noise model in their previous work [15], [16]. In this paper, unified models are developed for gate-current noise and their cross-correlation with the new expressions of effective gate overdrive, which is presented in Section II. The proposed models are accurate and continuous from weak- to strong-inversion regions. Besides, new analytical models are derived for the induced gate noise and the cross-correlation term of weakly inverted MOSFET. These simple expressions not only serve as the asymptotic limit for the validation of the proposed unified models, but also provide a clearer insight into and better understanding of the gate noise behavior in the weak-inversion region, which earns more far-reaching concerns lately. In Section III, the model parameter-extraction method by utilizing small-signal analysis, which is suitable for the common source–bulk configuration, is presented. Together with the proposed models for gate-current noise and the noise cross-correlation, the previously proposed HF drain-current noise model, which includes the junction-induced drain-current noise, is extended for the detailed analysis of four noise parameters of deep-submicrometer MOSFETs, with an emphasis on the low inversion region. Meanwhile, since the bulk transconductance is small in the weak-inversion region, the substrate contribution [19] can be disregarded. In Section IV, the results obtained from the proposed noise models are verified with experimental results. A figure-of-merit is introduced to determine the optimum gate biasing point in order to offer high gain with low driving power and low operating noise.

II. MODEL FORMULATION

A. Drain-Current Noise

In the weak-inversion region, the drain-current noise is often given by the shot noise expression of [3]

\[
S_{id} = 2qI_{sat} \left( 1 + e^{\frac{V_{GS} - V_{th}}{nV_T}} \right)
\]

(1)

\[
I_{sat} = \frac{\mu_{ox} W}{L_{eff}} C'_{ox} (n - 1) v_{th} e^{\frac{V_{GR} - V_{GR'}}{nV_T}}
\]

(2)

where \(v_{th} = kT/q\) is the thermal voltage, \(n\) is the subthreshold slope factor, \(V_{GR} = V_{GS} - V_T\) is the gate overdrive, \(V_T\) =...
\( V_{TH} - \eta V_{DS} \) is the threshold voltage taking into account the drain induced barrier lowering (DIBL) effect [3], [20], and \( V_{oFF} = V_{T,nub} - V_{TH} \) is the offset voltage, which can be extracted from current–voltage characterization in the subthreshold region.

At HF, the noise level of the subthreshold region is observed to be much higher than the noise level predicted by (1), as reported by [13]–[16]. In fact, according to van der Ziel in [17], the shot noise in the p-n+ junction at HF can be expressed by

\[
S_i = 2q1 + 4KTg
\]

where \( 4KTg \) is the additional noise component, which originates from the back-and-forth motion of electrons across the junction, resulting in the incremental conductance \( g \). Nevertheless, such electron motion does not contribute to the net current flowing to the output terminal.

The drain-current noise of the MOSFET in the weak-inversion region can be viewed as a two-sided shot noise process, proven by [3]. Therefore, the HF drain-current noise in the weak-inversion region can be written as [16]

\[
S_{i,\text{d}} = 2q1_{\text{sat}}(1 + e^{-V_{BG}/\mu V_{TH}}) + 4KTg_{\text{sh}} + 4KTg_{\text{shb}}
\]

where \( g_{\text{sh}} \) and \( g_{\text{shb}} \) are the ac conductance of the source–bulk and drain–bulk junction that can be modeled as a capacitor \( C \) in series with a resistor \( R \). Thus, the HF drain-current noise of the MOSFET in the weak-inversion region with a common source–bulk configuration is described as [16]

\[
S_{i,\text{d}} = 2q1_{\text{sat}}(1 + e^{-V_{BG}/\mu V_{TH}}) + 4KT\left(\frac{\omega^2 C_0^2 R_0}{1 + \omega^2 C_0^2 R_0^2}\right)\left(\frac{1}{\sqrt{\Phi_i}} + \frac{1}{\sqrt{V_{DS} + \Phi_i}}\right)
\]

where \( C_0 = W^2 V_i^2 \) and \( R_0 = W \) are in \( FV^{1/2} \) and \( \Omega V^{1/2} \). The values of \( C_0, R_0 \), and built-in potential \( \Phi_i \) can be extracted from the small-signal analysis in Section III.

In order to ensure the drain-current noise model to be valid in both the subthreshold and super-threshold regimes, a unified model is developed as shown in (6) [16] as follows:

\[
S_{i,\text{d}} = \delta 4KT\left(\frac{W}{L_{\text{eff}}\mu_{\text{eff}} C_{\text{ox}}^2}\right) V_{G \text{T,eff}}
\]

\[
+ 4KT\left(\frac{\omega^2 C_0^2 R_0}{1 + \omega^2 C_0^2 R_0^2}\right)\left(\frac{1}{\sqrt{\Phi_i}} + \frac{1}{\sqrt{V_{DS} + \Phi_i}}\right)
\]

Here, \( V_{G \text{T,eff}} \) is the effective gate overdrive, expressed as [16]

\[
V_{G \text{T,eff}} = \frac{2nV_{th}\ln(1 + e^{-V_{BG}/2nV_{th}})}{1 + 2n e^{-V_{BG}/2nV_{th}}} + \frac{1}{V_{G \text{T}} \mu_{\text{eff}} C_{\text{ox}}^2} \]

\[
\theta = \frac{1 + e^{-V_{BG}/\mu V_{TH}}}{2\delta}
\]

\[
\delta = \frac{1 - u + u^2/3}{1 - u/2}
\]

\[
u = \alpha V_{\text{eff}} / V_{G \text{T,eff}}
\]

where \( L_{\text{eff}} \) is the gradual channel length [10], [11], \( \mu_{\text{eff}} \) is the field dependent effective mobility [6], and \( \alpha \) is the bulk charge coefficient. \( V_{\text{eff}} \) and \( V_{G \text{T,eff}} \) are the drain bias and the overdrive voltage smoothening function of BSIM4 [20].

In strong inversion, since \( V_{GS} > V_{TH} \), \( V_{G \text{T,eff}} \) approaches \( V_{G \text{T}} \), and (6) reduces to the strong-inversion channel thermal noise model of [5], [6],

\[
S_{i,\text{d}} = \delta 4KT\left(\frac{W}{L_{\text{eff}}\mu_{\text{eff}} C_{\text{ox}}^2}V_{G \text{T}}\right)
\]

\[
(11)
\]

**B. Gate-Current Noise**

Induced gate noise is the current noise flowing into the gate, which is caused by the thermal fluctuations in the channel coupling to the gate terminal through the gate capacitance [17]. In strong inversion, the spectral density of the induced gate noise can be expressed as [19]

\[
S_{i,g} = \delta_g 4KT\left(\frac{W}{L_{\text{eff}}\mu_{\text{eff}} C_{\text{ox}}^2}(V_{G \text{T}})^2\right)
\]

\[
(12)
\]

where \( \delta_g \) is the induced gate noise parameter, defined as

\[
\delta_g = \frac{A e^{2/5}}{B}
\]

where

\[
a = 1 + \frac{V_{DS \text{,eff}}}{V_{th}}
\]

\[
v = \frac{\alpha V_{G \text{T}}}{V_{G \text{T}}}
\]

Here, \( u \) is defined by (10) and is defined in [19].

In order to develop a unified induced gate noise model, which is valid in all operating regions, the effective gate overdrive of (7) is innovated as

\[
V_{G \text{T,eff}} = \frac{2nV_{th}\ln(1 + e^{-V_{BG}/2nV_{th}})}{1 + 2n e^{-V_{BG}/2nV_{th}}}
\]

\[
\theta = \frac{1 + e^{-V_{BG}/\mu V_{TH}}}{2\delta}
\]

\[
\delta = \frac{1 - u + u^2/3}{1 - u/2}
\]

\[
u = \alpha V_{\text{eff}} / V_{G \text{T,eff}}
\]

Applying \( V_{G \text{T,eff}} \) in (16) to the gate overdrive \( V_{G \text{T}} \) in (12) yields the single-region induced gate noise model of

\[
S_{i,g} = \delta_g 4KT\left(\frac{W}{L_{\text{eff}}\mu_{\text{eff}} C_{\text{ox}}^2}(V_{G \text{T}})^2\right)
\]

\[
(21)
\]

In strong inversion, since \( V_{GS} > V_{TH} \), \( V_{G \text{T,eff}} \) approaches \( V_{G \text{T}} \), and (21) approaches (12). In the weak-inversion region where \( V_{GS} < 2V_{\text{eff}} \), the function of \( \ln(1 + e^x) \) in the numerator of (16) approaches its first-order Taylor approximation, which is \( e^x \). Besides, the denominator \( 1 + x \) approaches \( x \). The induced gate noise in (21) reduces to its subthreshold limit of

\[
S_{i,g} = \frac{4KT\left(\frac{W}{L_{\text{eff}}\mu_{\text{eff}} C_{\text{ox}}^2}V_{G \text{T}}\right)^2}{4(n-1)\sqrt{V_{th}}(1 - e^{-V_{BG}/V_{th}})^3}
\]

\[
(22)
\]
This subthreshold model can be derived based on the elementary model of the noise current, which is coupled to gate by the gate–oxide capacitance from each segment of the channel, together with the elementary model of the channel conductance of MOSFETs biased in the weak-inversion region. The details of derivation are given in the Appendix, Section A.

The cross-correlation between the induced gate noise and the channel thermal noise in strong inversion is given as \[ S_{i_a} = \frac{4kT}{L_{\text{eff}}} \mu_{\text{eff}} C_{\text{gs}} V_{\text{GT}}^2 \] (23)
\[ \delta_{gd} = \frac{u^2}{2} + \frac{v^2}{2} \left(1 + \frac{u}{v}\right) \] (24)
where \( u \) and \( v \) are defined by (14), (10), and (15), respectively. For the cross-correlation to be valid in both weak and strong inversion, a single-region equation is developed as
\[ S_{i_a} = \frac{4kT}{L_{\text{eff}}} \mu_{\text{eff}} C_{\text{gs}} V_{\text{GT}}^2 \] (25)
In (25), the new effective gate overdrive is introduced to be
\[ V_{\text{GT}} = \frac{m + \frac{n}{4}(n+1)}{m + \frac{n}{4}(n+1)} \cdot \left(2V_D - 2V_{aw} + V_{th}\right) e^{-2V_D/V_{th}} + 2V_{aw} - V_{th} \] (26)
\[ \delta_{gd} = \frac{4kT}{L_{\text{eff}}} \mu_{\text{eff}} C_{\text{gs}} V_{\text{GT}}^2 \] (27)
where \( m \) is a parameter to improve the slope of \( S_{i_a} \) in the moderate-inversion region. The current \( I_{DS} \) is modeled as (B.4) in the Appendix, Section B.

In strong inversion, (25) reduces to (23). In the weak-inversion region, (25) reduces to its subthreshold asymptotic limit of (28), with the details of derivation given in the Appendix, Section A,
\[ S_{i_a} = \frac{jkT}{L_{\text{eff}}} \mu_{\text{eff}} C_{\text{gs}}^2 V_{\text{GT}}^2 \] (29)
\[ \delta_{gd} = \frac{1}{2} \left[ u^2 + v^2 \left(1 + \frac{u}{v}\right) \right] \] (30)

Gate resistance noise has been reported by [9] to be crucial for short-channel devices. With the gate resistance noise [21], the unified total drain-current noise model, total gate-current noise model, and the cross-correlation term are
\[ S_{i_a} = \frac{4kT}{L_{\text{eff}}} \mu_{\text{eff}} C_{\text{gs}} V_{\text{GT}}^2 \] (31)
\[ \delta_{gd} = \frac{u^2}{2} + \frac{v^2}{2} \left(1 + \frac{u}{v}\right) \] (32)

The model parameters can be extracted from the small-signal analysis presented in Section III.

### III. SMALL-SIGNAL MODEL AND NOISE PARAMETERS

Fig. 1 illustrates the small-signal equivalent circuit in the common source–bulk configuration, with proposed noise sources added to a noiseless core network. The junction network, consisting of junction capacitance \( C_{jd} \), and junction resistance \( R_{ab} \), is proposed to model the HF incremental drain–bulk junction conductance [15]. For MOSFETs with symmetrical structures, the source–bulk junction conductance is computed from the drain–bulk junction conductance with zero voltage across junction [15]. For other topologies, such as the common-gate stage and cascode stages, the proposed noise models may not be valid, and thus modification works similar to [22] are needed.

The capacitances such as \( C_{gs} \) and \( C_{gd} \) are added to describe the effective capacitance effects of the gate due to source and drain terminals, respectively. The resistance \( R_{g} \) is added to model the gate resistance [23]. The transconductance and the transcapacitance \( C_m - C_{dg} - C_{gd} \) describe the transport current and the charging current at drain due to the gate [24]. The transconductance \( g_m \) and the source-to-drain conductance \( g_{ds} \) can be extracted from the first-order derivative of \( I_{DS} \) in (B.4) with regard to \( V_{GS} \) and \( V_{PD} \), respectively. The capacitance \( C_{sd} \) represents the source-to-drain capacitance.

Based on the small-signal equivalent circuit in Fig. 1, the Y-parameters can be expressed as [24]–[28]
\[ Y_{II} = \frac{\omega^2 (C_{gs} + C_{gd})^2 R_g + j\omega (C_{gs} + C_{gd})}{1 + \omega^2 (C_{kg} + C_{kd})^2 R_g^2} \] (33)
With the analysis of the measured Y-parameters, the small-signal parameters can be extracted [27]–[29]. By using an nMOS with \( L = 0.13 \ \mu m \), \( W = 20 \ \mu m \), operating at HF under subthreshold conditions of \( V_{GS} = 0.1 \ V \) for instance, the extraction process is presented. To simplify the extraction process, an approximation of (38) is made,

\[
\omega^2 (C_{gs} + C_{gd}) R_g^2 \ll 1.
\]  

Thereafter, the gate-to-drain capacitance \( C_{gd} \) and the gate-to-source capacitance \( C_{gs} \) can be extracted from the slope of the plots of \( \Im(Y_{11}) \) versus \( \omega \) and \( \Im(Y_{11} + Y_{12}) \) versus \( \omega \), respectively, as demonstrated in Figs. 2 and 3. Meanwhile, the gate resistance \( R_g \) can be obtained by plotting \( \Re(Y_{11}) \) versus \( |\Im(Y_{11})|^2 \), as shown in Fig. 4, and acquiring the slope.

Fig. 5 shows \( \Im(Y_{21}) \) versus \( \omega \) with the slope of \( -\omega^2 (C_{gd} + C_{gs} R_g g_m) \), from which the capacitance \( C_{gd} \) can be determined. In the subthreshold region, lowering the gate bias reduces the channel conductance \( g_{ds} \) exponentially, while HF enhances the junction conductance, and results in \( g_{ds} \ll g_{th} \). Hence, by plotting \( \omega^2 / \Re(Y_{22} - Y_{aa}) \) against \( \omega^2 \), the resistance \( R_{jdb} \) and the capacitance \( C_{jdb} \) can be extracted from the slope and the \( y \)-intercept of the plot, respectively [15], as depicted in Fig. 6.

\[
\frac{\omega^2}{\Re(Y_{22} - Y_{aa})} = \omega^2 R_{jdb} + \frac{1}{C_{jdb}^2} R_{jdb}.
\]  

In order to extract the model parameters of \( R_0 \), \( C_0 \), and \( \Phi_1 \) in (5), \( R_{jdb}^2 \) versus \( V_{DS} \) is plotted in Fig. 7,

\[
R_{jdb}^2 = R_0^2 V_{DS} + R_0^2 \Phi_1.
\]  

\( R_0 \) is the square root of the slope \( \Phi_1 \), and can be computed from the \( y \)-intercept point divided by the slope. Thereafter, \( 1/C_{jdb}^2 \) versus \( (V_{DS} + \Phi_1) \) is plotted in Fig. 8. Here, \( C_0 \) can be determined by taking square root of the slope,
The source-to-drain capacitance $C_{sd}$ can be extracted from the slope of the plots of $\Im(Y_{22} + Y_{12} - Y_a - Y_{db})$ versus $\omega$, as demonstrated in Fig. 9.

In order to simulate the four noise parameters from the weak-to-strong inversion regions, the optimized values for the bias-dependent capacitances $C_{ge}$, $C_{gd}$, and $C_{dg}$ are described as

$$C_{gs} = \varepsilon_1 C_{ox} W L_{eff} \frac{e^{(m_C V_{GS} - V_{th})/2m_{th}}}{1 + e^{(m_C V_{GS} - V_{th})/2m_{th}}} + C_{ov}$$

where $C_{gs}, C_{gd}, C_{dg}$, and $C_{ov}$ are fitting parameters. $C_{ov}$ denotes the overlap capacitance.

IV. RESULTS AND DISCUSSION

Fig. 10 shows the device-under-test (DUT), which is an N-type MOSFET designed in the common source–bulk configuration, fabricated using GLOBALFOUNDRIES Singapore Pte. Ltd.’s 0.13-μm RF CMOS technology process. A two-port S-parameter and HF noise measurement were performed using the HP8510 network analyzer and ATN NP5B microwave noise
parameter system. The accuracy of the noise figure and noise resistance measurement is presented in the Appendix, Section D. A de-embedding process [30], [31] was performed on the measured S-parameters and noise parameters in order to eliminate parasitic effects from pads and interconnects. Thereafter the power spectral density of $S_{11}$, $S_{12}$, and $S_{12}^*$, has been extracted [32] from the de-embedded noise measurement data.

Fig. 11 compares the extracted values of the capacitances $C_{gs}$, $C'_{ds}$, and $C'_{dss}$, with the capacitance values calculated from the expressions of (42)–(44), respectively, across the gate bias, for

Fig. 12. Extracted (symbols) and simulated (lines) $Y$-parameters versus frequency of the nMOS at a different operation region of weak inversion ($V_{GS} = 0.1\, \text{V}$), moderate inversion ($V_{GS} = 0.4\, \text{V}$), and strong inversion ($V_{GS} = 1.2\, \text{V}$). Excellent match is acquired between the simulated and measured $Y$-parameters.
nMOS with channel length $L = 0.13 \, \mu m$ and channel width $W = 20 \, \mu m$. It can be observed that the computed data matches well with the extracted data. After that, the $Y$-parameters are computed utilizing (32)–(35), together with the capacitance expression of (42)–(44) and other extracted model parameters.

In Fig. 12, the calculated $Y$-parameters are verified with the measurement data in the frequency domain up to 25 GHz on the MOSFET with channel length $L = 0.13 \, \mu m$ and channel width $W = 20 \, \mu m$. The transistor is biased at different gate voltages of $V_{GS} = 0.1 \, V$, 0.4 V, and 1.2 V, which fall into weak, moderate, and strong inversion, respectively. Fig. 12 demonstrates that the modeled $Y$-parameters matches well with the measured data, showing that the small-signal model is accurate. Hence, it is suitable to apply the entire small-signal parameters in the calculation of the four noise parameters.

Fig. 13(a) and (b) compares the simulated and the measured drain-current noise $S_{id}$ versus gate bias and frequency, respectively. In Fig. 13(a), the proposed drain-current noise model with junction-induced drain-current noise and the conventional model without junction-induced drain-current noise are compared for different channel lengths of $L = 0.13 \, \mu m$, $L = 0.25 \, \mu m$, and $L = 0.50 \, \mu m$. It can be observed that the noise level in the subthreshold region is highly underestimated by the conventional shot noise model. There are some unique features of the drain-current noise in this region. In this region, the noise is independent of the gate bias and the channel length, as shown in Fig. 13(a), and exhibits a non-white-noise characteristic, as depicted in Fig. 13(b). Apparently, the conventional model cannot capture the above-mentioned unique characteristics. By including the additional component of the HF shot noise, which is called junction-induced drain-current noise in this work, the accuracy of the subthreshold noise model has been improved significantly. The proposed model of (6), which includes the junction-induced drain-current noise, shows excellent match with the measured data across gate biases from the weak- to strong-inversion region including the moderate-inversion region, as illustrated in Figs. 13. The proposed model is also successfully verified with measurement data across frequencies up to 25 GHz.

Fig. 14 shows the comparison of the simulated and the measured gate-current noise $S_{ig}$ of the nMOS with channel length $L = 0.13 \, \mu m$ versus gate bias in (a), versus frequency in (b), and versus drain bias in (c). Fig. 14(a) evaluates the simulation results obtained from different $S_{ig}$ models, which are (22), (12), (21), and (30). The piece-wise induced gate noise models of (12) and (22) are valid in their particular regions of interest only, which are the strong- and the weak-inversion region, respectively. By introducing the effective gate overdrive expression of (16), the new unified induced gate noise model of (21) has been developed to be continuous from the weak- to strong-inversion regions, as depicted in Fig. 14(a). The gate resistance indeed contributes a substantial amount of noise intensity to the gate terminal and dominates the gate-current noise in the strong-inversion region. Thus, the model accuracy in strong inversion can be improved by including the gate resistance noise. However, in the weak-inversion region, induced gate noise increase exponentially with the decrease of the gate bias, and it dominates over the gate resistance noise, as depicted in Fig. 14(a). This is because the transfer function from the local noise source in the channel to the gate terminal is inversely proportional to the drain current, and hence, rises exponentially with the decrease of the gate bias in the weak-inversion region. In Fig. 14(b), the gate-current noise in the weak-inversion region exhibits exactly the same frequency dependence as in the strong-inversion region, which is proportional to the square of frequency. Meanwhile, it can be seen that the gate-current noise is a weak function of drain bias, as illustrated in Fig. 14(c). Fig. 14 also exhibits that the proposed model of (30) can accurately predict the gate-current noise characteristic of MOSFETs in all biasing conditions and operating frequencies. Moreover, it is demonstrated that the proposed model of (30) provides excellent continuity and accuracy from the weak- to strong-inversion regions including the moderate-inversion region.

In Fig. 15, the measured and simulated cross-correlation $S_{i'd'}$ of the nMOS with channel length $L = 0.13 \, \mu m$ and channel width $W = 20 \, \mu m$ are compared in (a), the gate bias domain, in (b), the frequency domain, and in (c), the drain bias domain. Fig. 15(a) manifests the estimated $S_{i'd'}$ by (28), (23), (25), and
Fig. 14. Extracted (symbols) and simulated (lines) spectral density of the gate-current noise versus gate bias in (a) versus frequency in (b) and versus drain bias in (c) of the nMOS with $W = 20 \mu m$ and $L = 0.13 \mu m$. The proposed gate-current noise model of (29) is continuous and accurate from the weak- to strong-inversion regions, while attaining good agreement with measured data over different frequencies and different biasing conditions.

Fig. 15. Extracted (symbols) and simulated (lines) spectral density of the cross-correlation between gate-current noise and drain-current noise versus gate bias in (a), versus frequency in (b), and versus drain bias in (c) of the nMOS with $W = 20 \mu m$, $L = 0.13 \mu m$, and $V_{DS} = 1.2 V$. The proposed model of (30) is continuous and accurate from the weak- to strong-inversion region of NMOS, attaining a good match with measured data over different frequencies and different biasing conditions.

It can be seen that the model of (23) fails in the weak-inversion region. By utilizing the effective gate overdrive expression of (26), a new single-region model, which is (25), is developed to simulate the cross-correlation between the induced gate noise and the channel thermal noise for all region of operation. It can be observed that the noise correlation term due to gate resistance dominates in the total $S_{g_1g_2}$ particularly in the strong-inversion region. Nevertheless, it becomes negligible in the weak-inversion region, as compared to the cross-correlation term due to channel. The proposed model of (31) is a unified model with smooth transition and with good accuracy from the weak- to strong-inversion region including the moderate-inversion region, as depicted in Fig. 15(a). Fig. 15(b) and (c) shows
that the proposed model of (31) can accurately predict the characteristic of $S_{dr}$, and matches well with the measurement results in the frequency and drain bias domain, respectively.

The extracted and the modeled minimum noise figure $\text{NF}_{\text{min}}$ and normalized noise resistance $R_n$ versus frequency of the nMOS with channel length $L = 0.13 \, \mu m$ and channel width $W = 20 \, \mu m$, biased at $V_{GS} = 0.1 \, V$ and $V_{DS} = 1.2 \, V$, are presented in Fig. 16. To observe the effect of junction noise on HF noise parameters, the results of two cases are compared. In the first case, the junction-induced drain-current noise is excluded in the noise parameter calculation, and the drain-current noise reduces to the conventional model of $2qI_D$. In this case, $R_n$ is extremely underestimated with an incorrect frequency dependent of $1/\omega^2$. Moreover, the minimum noise figure $\text{NF}_{\text{min}}$ exhibits a nearly flat trendline across frequency instead of the increasing trend observed from the measurement data. Meanwhile, in the second case, the proposed noise model, which includes the junction-induced drain-current noise, is applied in the noise calculation. By comparing the two cases, it is clearly demonstrated that the incorporation of the junction noise results in significant improvement on the accuracy of the noise prediction in the weak-inversion region. The frequency-dependence characteristics of the minimum noise figure and the noise resistance can be captured by taking into account the junction-induced drain-current noise.

On the other hand, the noise parameters are investigated in the gate bias domain, as illustrated in Fig. 17. The noise figure at 50 $\Omega$ NF$_{40}$ and the normalized noise resistance $R_n$ versus gate bias are shown in Fig. 17(a) and (b). There is a clear discontinuity between the strong-inversion (SI) and the weak-inversion (WI) model. Apparently, neither the strong-inversion model, nor the weak-inversion model can produce accurate noise parameter results in the moderate-inversion region. Nevertheless, such electron motion does not contribute to the net current flow in the output terminal. Therefore, this component cannot be captured by the existing industry models, such as the BSIM4 model [20], which calculate the junction noise as $2qI$. The detail of the BSIM4 noise model is given in the Appendix, Section E. With the inclusion of the proposed junction-induced drain-current noise, the accuracy of the simulation results improve remarkably.

Fig. 18 manifests the extracted and the simulated noise parameters, which are (a) minimum noise figure $\text{NF}_{\text{min}}$, (b) normalized noise resistance $R_n$, and (c) optimum source admittance $Y_{opt} = G_{opt} + jB_{opt}$, versus gate bias of the nMOS with $L = 0.13 \, \mu m$, and $W = 20 \, \mu m$. The proposed unified noise model, which includes the junction-induced drain-current noise, offers accurate results in weak- and moderate-inversion regions.
different dimensions. Immense improvements in the weak-inversion region can be observed for both of the channel lengths. The capabilities of the proposed model in predicting the accurate noise performance, with excellent continuity, in the weak- and moderate-inversion regions, is demonstrated by the smooth simulation curves in Fig. 18. The proposed noise model gives accurate results throughout the weak- and moderate-inversion regions, is demonstrated by the smooth simulation curves in Fig. 18.

A figure-of-merit of \( FOM = \frac{g_m}{|I_{DS}|(N_{F_{min}} - 1)} \) is introduced to evaluate the ratio of gate transconductance to the biasing current and to the corresponding noise performance of the device. A device with high value of \( FOM \) is efficient in terms of driving power and operating noise. The performance metric \( FOM \) of the nMOS with different channel lengths are evaluated throughout the gate biases in Fig. 19. From the plot, the optimum biasing point \( V_{GS,\text{opt}} \), which offers high gain with low power and low noise, can be justified from the maximum \( FOM \) obtained. The way of determining the optimum gate bias is essentially useful for the application in low-power low-noise RF design. As illustrated in Fig. 19, the peak of the \( FOM \) slightly shifts to the lower value of \( V_{GS,\text{opt}} \), from 0.46 to 0.43 V with channel lengths decreases from 0.50 to 0.13 \( \mu \)m. The optimum gate biases for all the channel lengths fall in the moderate-inversion region, where both of the strong- and weak-inversion noise models would fail. It is demonstrated that the proposed unified noise model, which is continuous and accurate for all regions of operation, gives an accurate prediction on the above-mentioned \( FOM \) and on the optimum value of gate bias. From Fig. 19, it can be observed that the values of \( FOM \) for 0.25-\( \mu \)m nMOS is 2.5 times higher than the values for 0.50-\( \mu \)m NMOS. As the channel length reduces from 0.50 to 0.13 \( \mu \)m, the performance metric increases ten times. This indicates that the improvement on the performance metric becomes more prominent with continued down-scaling.

V. CONCLUSION

In this paper, new unified \( V_T \)-based models for HF drain-current noise, gate-current noise, and their cross-correlation have been presented. The model development is based on the common-source–bulk configuration aligned with the DUT fabrication. The subthreshold model for induced gate noise and its cross-correlation with channel thermal noise has been derived to offer an insight into and understanding of the noise performance of the MOSFET in weak inversion. With the proposed effective gate overdrive expression, the unified noise models, which provides excellent continuity from weak- to strong-inversion regions, are developed and are proven to merge with their asymptotic models in weak and strong inversion. With incorporation of the junction-induced drain-current noise, the accuracy of subthreshold noise parameters improves remarkably. The proposed models have been demonstrated to
be continuous and accurate with excellent match to experimental data for different frequencies up to 25 GHz and different biasing conditions including the weak- and moderate-inversion regions. The proposed noise models are particularly useful in finding the optimum point of gate bias to offer high gain with low driving power and having good noise performance at the same time. Hence, the proposed models are important in low-voltage low-power RF applications.

**APPENDIX**

A. Derivation of Induced Gate Noise and Its Cross-Correlation With Channel Thermal Noise in Weak Inversion

The noise current coupled by the gate–oxide capacitance from each small segment of the channel is derived as [17]

\[ \Delta i_g = j\omega WC_{ox} \Delta i_D \left( -\int_0^{V_D} \frac{y}{g(V)} \, dy + \int_{V_D}^{V_C} \frac{L}{g(V)} \, dy \right). \]  
(A.1)

Since \( I_D = g(V)(dV/d_y) \),

\[ dy = \frac{g(V)}{I_D} \, dV. \]  
(A.2)

For MOSFETs operating in the weak-inversion region, the channel conductance is given as [3], [17]

\[ g(V) = \mu W V_{th} (n-1) C_{ox} e^{(V_{GSS} - V_{th})/nV_{th}} e^{-V_i/V_{th}} \]  
(A.3)

Thus,

\[ y = \int_0^{V} \frac{g(V)}{I_D} \, dV = \frac{L(1 - e^{-V_i/V_{th}})}{1 - e^{-V_D/V_{th}}}. \]  
(A.4)

Substituting (A.2)–(A.4) into (A.1) yields

\[ \Delta i_g = j\omega WC_{ox} \frac{L}{I_D} \Delta i_D (V_{aw} - V_y) \]  
(A.5)

\[ V_{aw} \equiv V_{th} + V_D - \frac{V_D}{1 - e^{-V_D/V_{th}}}. \]  
(A.6)

The power spectral density \( S_{i_g} \) and \( S_{i_g i_g^*} \) are then given by

\[ S_{i_g} = \frac{4kT \omega^2 W^2 C_{ox}^2}{I_D^3} \int_0^{V_C} g^2(V_{aw} - V_y) \, dV_y. \]  
(A.7)

\[ S_{i_g i_g^*} = 4kT \frac{j\omega WC_{ox}^2}{I_D^2} \left( \frac{W}{L} \right) \int_0^{V_C} g^2(V_{aw} - V_y) \, dV_y. \]  
(A.8)

Substituting (A.3)–(A.7) yields (22). Substituting (A.3)–(A.8) yields (28), or its alternate form can be written as

\[ S_{i_g i_g^*} = 4kT j\omega W C_{ox}^2. \]  
(A.9)

\[ \epsilon = \left( \frac{1}{V_{th}(1 - e^{-V_D/V_{th}})^2} \right) \left[ (2V_D - 2V_{aw} + V_{th}) e^{-V_D/V_{th}} - (-2V_{aw} + V_{th}) \right]. \]  
(A.10)

B. Unified Drain-Current Model

The piece-wise current models for strong and weak inversion are often obtained by (B.1) and (B.2), respectively,

\[ I_{DS,ST} = \frac{\mu_{eff} C_{ox}}{I_{eff}} (V_{GS} - V_T) V_{de} \]  
(B.1)

\[ I_{DS,ST} = \frac{\mu_{eff} C_{ox}}{I_{eff}} V_{th}^2 (n-1) e^{(V_{C-T} - V_{th})/nV_{th}} - (1 - e^{-V_D/V_{th}}) \]  
(B.2)

where

\[ V_{de} = V_{doff} \left( 1 - \frac{y}{2} \right). \]  
(B.3)

Thus, a unified model for current \( I_{DS} \) is required for (25). The one-region model for current \( I_{DS} \) in [33] is modified to be (B.4) to improve the slope of \( I_{DS} \) in the moderate-inversion region

\[ I_{DS,ST-W} = \frac{\mu_{eff} C_{ox}}{I_{eff}} V_{gg} V_{ge} \]  
(B.4)

\[ V_{gg} = \frac{nV_{th} \ln(1 + e^{m* V_{C-T} / nV_{th}}) V_{de}}{m^* + V_{de} e^{-[(1-m^*) V_{C-T} - V_{th}]/nV_{th}}} \]  
(B.5)

\[ W_{ge} = 1 - \frac{2m^* \alpha}{n} e^{-[m^* V_{C-T} - V_{th}] (1 - e^{-V_D/V_{th}})}. \]  
(B.6)

Here, \( m^* \) is a fitting parameter defined by BSIM4 [20].

C. Four Noise Parameter Model

The noise factor \( F \) is defined as [34]

\[ F = \frac{(S/N)_m}{(S/N)_{cut}} \]  
(C.1)

where \( S \) denotes the signal power and \( N \) is the noise power. Noise figure \( NF \) is an equivalent form of noise factor in decibels (dB),

\[ NF = 10 \log_{10} F. \]  
(C.2)

The noise factor can be expressed in terms of the four noise parameters, given as [27]

\[ F = F_{min} + \frac{|Y_s - Y_{opt}|^2 R_n}{G_s}. \]  
(C.3)

Based on two-port network theory, the four noise parameters of MOSFETs calculated using the small-signal equivalent circuit in Fig. 1, can be written as [19], [30], [35], [36]

\[ R_n = H \frac{S_{i_g}}{4kT T_{21}^2}. \]  
(C.4)

\[ G_{cor} = \Re(Y_{11}) + \frac{S_{i_g i_g} \Re(Y_{21})}{4kTR_n Y_{21}^2}. \]  
(C.5)

\[ B_{opt} = -B_{cor} - \Im(Y_{11}) \frac{S_{i_g i_g} \Re(Y_{21})}{4kTR_n Y_{21}^2}. \]  
(C.6)

\[ |Y_{opt}|^2 = \frac{S_{i_g}}{4kT R_n} + \frac{|Y_{11}|^2 - 2 \Re(Y_{11}) \Im(Y_{11}) - G_{cor}}{2 \Im(Y_{11}) \Re(Y_{11}) - B_{cor}} \]  
(C.7)
Alternatively, the noise parameters can be expressed by using the three-parameter "PRC" model [37],

\[ R_n = P \cdot g_m Y_{21} \]  \hspace{1cm} (C.10)
\[ G_{cor} = \Re(Y_{11}) + \Im(Y_{21}) \left[ \omega \sqrt{\frac{C_{gs}}{g_m}} \left( \frac{C}{P} \right) \right] \]  \hspace{1cm} (C.11)
\[ B_{opt} = -\Im(Y_{11}) + \Re(Y_{21}) \left[ \omega \sqrt{\frac{C_{gs}}{g_m}} \left( \frac{C}{P} \right) \right] \]  \hspace{1cm} (C.12)

\[ |Y_{opt}|^2 = \frac{\omega^2 C_{gs}}{g_m} Y_{21} \left[ \frac{R}{P} \right] + |Y_{11}|^2 \]
\[-2 \left[ \omega \sqrt{\frac{C_{gs}}{g_m}} \left( \frac{C}{P} \right) \right] \cdot [\Re(Y_{11})\Im(Y_{21}) + \Im(Y_{11})\Re(Y_{21})] \]  \hspace{1cm} (C.13)

where \( P \) is the drain noise coefficient, \( R \) is the gate noise coefficient, and \( C \) is the correlation noise coefficient

\[ P = \frac{S_{td}}{4kTg_m} \]  \hspace{1cm} (C.14)
\[ R = \frac{S_{tg}g_m}{4kTw^2C_{gs}} \]  \hspace{1cm} (C.15)
\[ C = -\frac{S_{t\phi}^*}{\sqrt{S_{td} \times S_{tg}}} \]  \hspace{1cm} (C.16)

Here, \( S_{td} \) and \( S_{tg} \) are given by (29) and (30). \( g_m \) is obtained from the first-order derivative of \( I_{DS} \) in (B.4). \( C_{gs} \) can be obtained from (42).

D. Noise Measurement: Margin of Error

Fig. D.1 shows the extracted minimum noise figure \( NF_{m,n} \) and normalized noise resistance \( R_n \), with error bars, versus gate bias, of nMOS biased in the low inversion region. The error of noise figure in low inversion is less than \( \pm 1.8 \) dB, and the error of normalized noise resistance is less than \( \pm 5.2 \). Since it is extremely difficult to measure noise parameters accurately in the subthreshold region, where the small transistor has a small gain in a 50-\( \Omega \) system like the ATN NP5 system, the averaging method is adopted to minimize the measurement errors and fluctuations, and to ensure the accuracy of the measurement data.

E. BSIM4 Noise Model

Fig. E.1 shows the subcircuit-based MOSFET representation with BSIM4 as the core model and the junction diodes with the current noise source added. In the existing industry models, such as the BSIM4 model [20] and PSP JUNCAP2 [38] model, the current noise of diode is modeled as [20], [38]

\[ S_{I_{d,jd}} = 2qI_{D_{jd}} \]  \hspace{1cm} (E.1)
\[ S_{I_{d,jb}} = 2qI_{D_{jb}} \]  \hspace{1cm} (E.2)

where \( I_{D_{jd}} \) and \( I_{D_{jb}} \) are the dc leakage currents of the drain–bulk and source–bulk junction diodes. The leakage currents are very small, and thus the current noise of the diode is negligible as compared to the drain-current noise found in the subthreshold region.

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