A 35 mW 30 dB Gain Control Range Current Mode Programmable
Gain Amplifier With DC Offset Cancellation

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Abstract — A 6-bit programmable gain amplifier (PGA) with current mode exponential gain control is presented in this paper that achieves a linearity error within ±0.1 dB over a 30-dB wide gain control range. The proposed design topology has two digitally-variable gain amplifiers and a post amplifier that are interconnected by a differential pair wideband matching network to provide an enhanced gain bandwidth product. The proposed PGA has 35 mW power consumption and occupies 0.25 mm² core die area.

Index Terms — Current mode design, DC offset cancellation, exponential current converter, linear-in-decibel, programmable gain amplifier, SiGe BiCMOS, variable gain amplifier.

I. INTRODUCTION

The RF transceivers designed for mobile communication, due to the varying distance between transmitter and receiver, result in the signal strength fluctuations at the receiver antenna. The maximum signal level fluctuation is the dynamic range that the receiver frontend circuits must handle without distortion caused by either the saturation of a strong signal or desensitization by the noise floor on a weak signal. The automatic gain control (AGC) at the end of the receiver chain prevents the propagation of the signal fluctuations to the baseband circuit and hence reduces the dynamic range requirement at the baseband circuitry. To improve the settling time and tuning range of the AGC, an exponential gain control is desirable which can be accomplished by using a linear-in-decibel analog variable gain amplifier (VGA) [1]-[3] or a linear-in-decibel programmable gain amplifier (PGA) [4] in the AGC loop. The dB-linear gain control in the conventional VGA is achieved by using bipolar junction transistors (BJT) based on the control voltage that consumes more power exponentially without limiting the rail-to-rail DC current. In addition, it is difficult to achieve a precise on-chip voltage reference that provides high accuracy dB-linear characteristic.

The proposed PGA, by using current mode exponential gain control provides a precise linear-in-decibel gain control with linearity error within ±0.1 dB over a wide 30 dB gain control range and the current mode biasing directly limits rail-to-rail DC current and reduces the overall DC power consumption. Additionally, the proposed design topology has a low loss interconnect stage that improves the overall gain-bandwidth product (GBW) and a fixed gain post amplifier that provides a nearly gain-independent output gain compression point which is desirable in the RF receiver frontend to provide a stable drive power level to the baseband over a wide dynamic range.

This paper presents the design and on-wafer measurement results of the proposed PGA.

II. CIRCUIT DESIGN DESCRIPTION

The block diagram of the proposed PGA shown in Fig. 1 consisting of two digitally-variable gain amplifiers (DVGA) core stages, a post fixed gain amplifier and the RC parallel interconnect network pair that allow differential AC coupling.

The circuit schematics of the DVGA core and the post amplifier have different current biasing circuit (IBIAS) as shown in Fig. 2. The schematic of either the DVGA core or the post amplifier consists of three differential stages that are biased using current mirrors (Vbias2) from a bandgap reference to obtain a low power design. The intermediate stage is the core amplifier (Q5,6) with feed-forward DC offset canceller (DCOC) and its gain is determined by the IBIAS current source. For the DVGA core, the IBIAS current source consists of a NMOS based digital to analog current converter (BX[X:0:5]) to ICTRL, and a BJT based exponential current converter (ICTRL to IET) that is designed to provide a precise linear-in-decibel
gain control. In addition, the post amplifier has a fixed current source (M8,9) providing a measured gain of +16 dB. The post amplifier presents a high output 1-dB gain compression point (PldB) over the entire PGA gain tunable range to meet the 150-mVpp signal level requirement from the baseband. The input stage (Q1,2) with the transimpedance load (Q3,4) and the output stage (Q7,8) are responsible for providing a differential wideband 50-Ω impedance matching with fixed common mode DC voltages that are independent of the PGA gain control. The proposed PGA has a bandwidth starting from 3

MHz due to the DCOC and an upper cutoff frequency of 1.7 GHz providing ±0.75 dB gain flatness to support a channel bandwidth of 1.08 GHz with protection band based on the IEEE 802.11ad standard. The interconnect network included in the proposed PGA is a preferred choice for this design scenario.

The interconnect network is a crucial circuit to keep good matching with low loss for cascading any two adjacent stages. We introduce the RC network in Fig. 1(c) for the integration of the multiple amplifier stages. Based on the investigation, the interconnect network can:

1) ensure the overall PGA's GBW (by introducing a zero at \[2\pi(R + R_{cap})C\] before the PGA lower cutoff frequency = 3MHz) close to sum of GBW of each stage,

2) provide low insertion loss at the PGA operating frequency range (via the capacitor C beyond f2 frequency),

3) ensure ±0.75dB gain flatness without gain peaking and good wideband differential matching (with nearly 0-Ω interconnect impedance beyond f2),

4) accommodate different optimized DC voltages between the amplifier stages (as the DC voltage difference drops across the resistor R) unlike the fixed voltage of the direct coupling and the power hungry active level shifter, and

5) have the smaller size (reducing the decoupling capacitor dimension by R times) compared with the decoupling capacitor alone.

A relatively large resistor value (R) is desirable to drop a large DC voltage difference between adjacent stages without loading, that moves the zero to lower frequency based on \[2\pi(R + R_{cap})C\]−1. The increased R value results in larger insertion loss in the range from DC to 2 MHz and almost does
not affect the PGA passband frequency response due to the lower cutoff frequency predetermined by the DCOC. The low loss interconnect structure can preserve the overall GBW product when number of baseband amplifier stages need to be increased to meet high gain control range required by the baseband. Hence the value of resistor R provides a degree of design freedom to choose the DC biasing voltages between the PGA stages that ensures better amplifier performance of each of the PGA stages.

### III. Experimental Results

The die micrograph of the proposed PGA with the on-chip bandgap reference shown in Fig. 3 is implemented in 0.18 μm SiGe BiCMOS process. The PGA performance is measured by on-wafer probing and it occupies 0.25 mm² active die area (excluding measurement pads). The measured S-parameters shown in Fig. 4 indicates a 30 dB fine gain control range with ±0.75 dB gain flatness over 1.2 GHz and a gain independent input/output return loss better than 13 dB over the entire operating frequency range.

Fig. 5 and Fig. 6 depicts the measured P1dB for maximum and minimum PGA gain, respectively. The plots indicate that the proposed PGA is capable of driving a constant differential drive power level better than -10 dBm (0.2-Vpp) over the entire gain control range. This is achieved by incorporating a fixed high gain post amplifier. Hence the designed PGA can improve the sensitivity of the RF receiver frontend as well as the overall transceiver dynamic range by interfacing with digital baseband to form a complex reconfigurable AGC (as shown in Fig. 1) that dynamically regulates the power level to the baseband input.

Table I summarizes the measured performance of the proposed design along with the state-of-the-art works. As compared to the state-of-the-art VGAs with comparable gain range [1]-[3], that make use of voltage mode for biasing and gain control, the proposed design by using the current mode exponential gain control has enhanced linear-in-decibel performance (linearity error ≤ ±0.1 dB) and the current mode biasing reduces the overall DC power consumption by limiting the rail-to-rail current to 19.4 mA from a 1.8-V supply. Unlike the analog mode state-of-the-art VGAs [1]-[3], the proposed PGA is compact in size and can be directly interfaced with the digital baseband without the need for additional DAC.

### Table I

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Technology</td>
<td>0.18 μm SiGe</td>
<td>0.18 μm CMOS</td>
<td>90 nm CMOS</td>
<td>0.13 μm SiGe</td>
<td>0.18 μm SiGe</td>
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<td>Gain control range</td>
<td>-1.4 to +30.2 dB</td>
<td>-37 to +21 dB</td>
<td>19 dB</td>
<td>-10 to +30 dB</td>
<td>-10.6 to +7.8 dB</td>
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<tr>
<td>Maximum linearity error</td>
<td>±0.1 dB</td>
<td>±1 dB</td>
<td>-</td>
<td>±0.3 dB</td>
<td>±0.1 dB</td>
</tr>
<tr>
<td>3-dB Bandwidth</td>
<td>3 M to 1.7 GHz</td>
<td>10 GHz</td>
<td>22 GHz</td>
<td>0.2 M to 7.5 GHz</td>
<td>2 M to 1.9 GHz</td>
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<tr>
<td>Power consumption</td>
<td>35 mW</td>
<td>54 mW</td>
<td>75 mW</td>
<td>72 mW</td>
<td>12.2 mW</td>
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<tr>
<td>Supply voltage</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.2 V</td>
<td>1.2 V</td>
<td>1.8 V</td>
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<tr>
<td>Active core area</td>
<td>0.25 mm²</td>
<td>1.32 mm²</td>
<td>0.56 mm²</td>
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<td>0.048 mm²</td>
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<td>Output voltage swing</td>
<td>200 to 266 mVpp $</td>
<td>394 to 450 mVpp</td>
<td>520 mVpp</td>
<td>35 mVpp</td>
<td>47.9 to 323 mVpp $</td>
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<tr>
<td>Gain control mode</td>
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<td>Analog</td>
<td>Analog</td>
<td>Analog</td>
<td>Digital</td>
</tr>
</tbody>
</table>

$^*$Based on output 1dB gain compression (P1dB) point

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![Fig. 5. Measured P1dB for maximum PGA gain at 1 GHz.](image1)

![Fig. 6. Measured P1dB for minimum PGA gain at 1 GHz.](image2)
the state-of-the-art PGA [4] has improved gain control linearity, small die size and reduced power consumption, the proposed PGA achieves same linearity performance over a larger gain control range. Additionally, the proposed design has small variation in the output voltage swing over the complete gain control range, contrasting the PGA in [4].

IV. CONCLUSION

This paper proposes a PGA that uses exponential current converter to achieve a 30 dB precise linear-in-decibel digital gain control with a gain error less than ±0.1 dB. This work uses the current mode approach along with a multi-purpose interconnect network to provide state-of-the-art performance that can be used in low power RF receivers to interface with the baseband.

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REFERENCES