A Miniaturized 28mW 60GHz Differential Quadrature Sub-Harmonic QPSK Modulator in 0.18um SiGe BiCMOS

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Abstract—A new sub-harmonic QPSK architecture is proposed for microwave and millimeter-wave applications including transceiver. The developed 60GHz differential quadrature sub-harmonic QPSK modulator based on the proposed new QPSK architecture can not only reject both the image frequency and LO leakages but also reduce the LO operation frequency to the half of the conventional modulator. Moreover, the proposed QPSK modulator provide flexibility to select either the low sideband (LSB) or upper side band (USB) and support data rate as high as 3.52Gbps. The compact chip size is only 400umx300um and power consumption of 28mW is much smaller as compared to that of the state of the arts.

Index Terms — Millimeter-wave, QPSK Modulator, RFIC, Baseband, Harmonic, IEEE802.11ad, 60GHz, BiCMOS

I. INTRODUCTION

Frequency conversion or modulation from baseband (BB) is crucial for millimeter-wave wireless communication since the BB normally operates in lower frequency or the GHz frequency range while RF frequency is in mm-wave frequency range [1-5]. The simple way to do the conversion from BB to mm-wave is to directly modulate the BB digital to mm-wave. For 60GHz application, the BB input bandwidth is normally from DC up to 1.08GHz according to the channel bandwidth of 2.16GHz at 60GHz, while the data rate can be up to multiple Gbit/s [4]. The interfaces from BB are preferred to be differential quadrature signals with up conversion for simplifying the BB processing especially for the high speed communication system. While after up-conversion, the unwanted sidebands and local oscillator (LO) frequency are very close to the desired signals at 60GHz. In order to reject the unwanted signals, the up-conversion modulator with an image and LO reject capability is preferred. With broadband matched IF input port and LO leakage to RF and IF ports, the DC offset also become an issue for direction conversion modulation scheme.

Based on the constraint consideration for mm-wave applications, we propose a new differential quadrature sub-harmonic QPSK modulator architecture, which use the proposed miniaturized differential IQ converter (DIQC) coupler and compensation hybrid coupler. It can not only reject both the image frequency and LO leakages but also reduce the DC offset by reducing the LO operation frequency to the half of the conventional modulator. Moreover, the modulator provides flexibility to select either the low sideband (LSB) or upper side band (USB). Moreover, as compared with that of the state of the arts [2-3], the QPSK modulator provides the smallest size and the lowest power consumption beside the image rejection capability.

II. APPLICATION AND SCHEMATICS

Fig.1 shows the proposed 60GHz transceiver system based on the sub-harmonic modulator and demodulator for 60GHz applications. The frequency synthesizer operating around 30GHz is shared as LO drive for either/both transmitter and/or receiver. The passive differential IQ converter (DIQC) is used to convert the differential LO signals from synthesizer to the differential quadrature LO signals i.e. LO_0, LO_90, LO_180, LO_270. For practical application, the DIQC together is integrated with the modulator/ demodulator for better phase and amplitude balance and image rejection. The scheme can also give additional option to choose either low side band (LSB) modulation or upper side band (USB) conversion. For USB preferred case, the LSB is connected to 50ohm load and vice versa. The transceiver architecture with half LO operating...
frequency of fundamental architecture can directly convert between RF and analog/digital baseband with image rejection capability by only adding LNA/PA at 60GHz input/output respectively. Thus it reduces the number of the components, chip area and total power consumption by simplifying Tx/Rx Chain as well as LO chain by low down the LO operation frequency to the half.

Fig. 2 shows the schematic the proposed differential IQ sub-harmonic modulator with image rejection. The transistors Q1–Q8 are MOS transistors. PMOS Q2, NMOS Q1 and resistor R1 are connected as inverter to form the IF/data amplifier with low pass response, which can also improve the rejection of the RF and LO leakage. Four inverters, connected to IF_0, IF_90, IF_180 and IF_270, are formed by Q1–Q8 and R1–R4. Transistors M1–M8 are BJTs, which can provide as high as 200GHz for the nonlinear 60GHz operation. BJT M1 and M2 form the differential drive transistor pair, which will operate at frequency double as well as nonlinear mixing of LO and IF/data. There are four transistor pairs are formed. For harmonic conversion operation, The LO drive signals of LO_0, LO_90, LO_180 and LO_270 are preferred to be the same amplitude and different phase of 0, 90, 180, 270 degrees respectively. The base current for each BJT is provided by the on-chip bandgap current source with total current about 19uA shared by 8 BJTs. DC block capacitor C3–C6 are used to make sure the “base” current bias while feed through the LO drive signals. The on chip 60GHz broad band 90 degrees hybrid is developed with compensated balance in phase and amplitude to combine the orthogonal vector signals to either LSB or USB with image rejection capability. The required four-phase LO signals of LO_0, LO_90, LO_180 and LO_270 can be provided by differential quadrature VCO, which consumes more power as compared to differential VCO. Here we propose a broad band passive differential IQ network to convert from differential LO to differential IQ LO. The proposed sub-harmonic modulator was designed by using Jazz Semiconductors’ SBC18H2 SiGe process with 6 aluminum metal layers, MIM capacitors, and inductors using 2.8μm thick aluminum top metal layer and 2μm thick top via layer. The simulation is performed both in ADS2009 simulator as well as in the cadence Spectra RF simulator.

III. PERFORMANCE SUMMARY

The results and the photographs of the designed 90 degree hybrid with balance compensation and DIQC are given in Fig.3. The hybrid measured low insertion loss of 1.5dB while the amplitude and phase balance are less than 0.8dB and 2 degrees from 40 to 66GHz. The simulated results of the 8-port DIQC show the better than -15dB input return loss and isolation from port 1 to port 2 in the frequency range 20–40GHz under differential drive of the four pair differential drive ports. When the input port 1 under differential drive and isolation port 4 with 100Ω load, the output differential ports port 3 and port 4 will provide differential outputs with 90 degrees phase difference.
The balance characteristics in terms of both amplitude and phase to the transistors are crucial for the good LO, 2LO and image rejection of the modulator, the full EM simulation is carried out to count in all interconnects in EM simulation results. The measurement of the proposed sub-harmonic modulator is carried out by using the probe station from CASCADE and the equipment Agilent E5052B signal source analyzer along with the Agilent harmonic mixer 11970A (low band) and 11970V (high band). Figure 4 shows the die photograph of Sub-harmonic Modulator under test.

The measured results of the hybrid are shown in Figure 3. The Amplitude error is less than 0.8dB and the Phase error is less than 2 degrees. The simulation results of the differential drive 4ports are also shown in Figure 3. The Amplitude error is less than 0.8dB and the Phase error is less than 2 degrees. The measurement of the proposed sub-harmonic modulator is carried out by using the probe station from CASCADE and the equipment Agilent E5052B signal source analyzer along with the Agilent harmonic mixer 11970A (low band) and 11970V (high band). Figure 4 shows the die photograph of Sub-harmonic Modulator under test.

### Table 1: System Specifications

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>[2]</th>
<th>[3]</th>
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<tr>
<td>Process</td>
<td>SiGe 0.18um</td>
<td>SiGe 0.12um</td>
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<tr>
<td>Die Size</td>
<td>400um x 700um</td>
<td>400um x 300um w/o DIQC</td>
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<td>IF ports</td>
<td>Differential &quot;I&quot; and &quot;Q&quot;</td>
<td>Differential &quot;I&quot; and &quot;Q&quot;</td>
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<td>8.3~9.1GHz</td>
<td></td>
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<tr>
<td>RF BW</td>
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<td>57~64GHz</td>
<td>59~66GHz</td>
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<td>-20dBc</td>
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<tr>
<td>IF@RF</td>
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<td>-</td>
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<td>2LO@RF</td>
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<td>-</td>
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<td>N.A&gt;</td>
<td>2LO-IF@RF -20</td>
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<td>19.2mA, 2.7V</td>
<td>75.9mW</td>
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photograph of sub-harmonic modulator under test. Under current consumption of 15.3 mA from a 1.8V supply, the modulator achieves a flat conversion gain frequency response of $5=-0.5$dB over 57GHz to 66GHz, an input P1dB of -14dBm, sideband rejection greater than 15dBc, and LO and 2LO suppression of more than 28dBc. The modulator area is only 400um by 300um for the QPSK modulator core and 700um by 400um including passive DIQC. The results of this modulator are compared with the state of the art in Table I. It can be seen that the proposed modulator show advantages in terms of the image rejection, size and power consumption.

Figure 5 shows the results of the modulator under QPSK modulation condition. The differential “I” and “Q” digital square wave signals are input to the proposed sub-harmonic modulator, the output 60GHz spectrum is down converted to 5GHz for analyzing by digital analyzer. The results show that the modulator can support 3.52Gbps data (limited by the equipment). The non-ideal constellation and eye-diagram may be due to the unbalance off-chip drive signals of LO and IF in the test system.

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REFERENCES