V-Band High Gain SiGe Power Amplifier with Wideband ESD Protection

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Abstract—This paper presents a low-power high-gain V-band power amplifier (PA) in a low-cost commercial 0.18-μm SiGe BiCMOS technology. A novel wideband ESD protection circuit is demonstrated with <1 dB insertion loss in frequency range of 17-88 GHz. Design techniques utilized to optimize the gain and the power consumption are addressed. In the 60GHz frequency range, the designed PA achieves a peak gain of 20.8 dB under 1.8 V supply and 25.3 dB under 2.4 V supply respectively. The input return loss is better than -10 dB from 50 GHz to 75 GHz. It delivers 8.4 dBm saturated output power at 67 GHz with a 2.4 V supply. TLP measurement result shows that the voltage is clamped below 6 V even under 10 A ESD current.

Keywords—SiGe BiCMOS; millimeter-wave; power amplifier; ESD; V-band

I. INTRODUCTION

The unlicensed 9 GHz spectrum at V-band (50-75 GHz) presents a great opportunity for high speed short range wireless communication [1]. The development of low cost high performance power amplifiers (PAs) for such high frequency is still a challenge due to low power gain, low break down voltage, low resistivity substrate and low-Q on-chip passive components especially at V-band. Recently, SiGe BiCMOS technology has been proved as a suitable technology to satisfy both the millimeter-wave frequency and cost requirements, especially with its potential of large scale integration [2].

Recent reported PAs have been developed to increase the saturated output power (P_{sat}) and power added efficiency (PAE) [3]-[6]. Conventional common-source cascode V-band PA with 15 dBm P_{sat} and 20% peak PAE under 2.4 V supply has been demonstrated in [3]. A differential push-pull PA in 0.13-μm SiGe BiCMOS process [4], which can deliver 20 dBm and 12.7% peak PAE is reported. The transformer-coupled PA based on 2-way power combination in [5] using 65-nm CMOS process achieved 14.9 dBm Psat and 16.2% peak PAE. N-way (N=2) power combine technique such as distributed active transformer topology has proved to achieve P_{sat} up to 23 dBm at 60 GHz in 0.13-μm SiGe BiCMOS process [6]. However, these PAs in [3]-[6] are designed with high power consumption so as to increase the P_{sat} and PAE performances. The low power consumption and the good ESD protection capability should be taken into account for low-cost commercial consumer products. A coplanar waveguide (CPW) ESD co-design using an inductive cancellation method was introduced in low noise amplifier design [7]. However, The CPW ESD is based on shunt stub, which has narrow RF bandwidth.

In this paper, a low-power high-gain V-band PA with novel frequency independent wideband ESD is proposed to cover the 17-88 GHz frequency range without significantly sacrificing the RF performances, such as impedance matching and power gain flatness. The size of proposed ESD is independent to the operation frequency. The optimization for low-power and high-gain PA is discussed and addressed. The proposed PA is optimized to support two channels from 61.56 GHz to 65.88 GHz, compatible with the WirelessHD and 801.11ad (WiGig) standards.

II. POWER AMPLIFIER DESIGN

A. Power Amplifier Design

Fig.1 shows the schematic of the proposed four-stage PA (the bias bypass circuits are not shown). There is a trade-off between power consumption and power gain. The major challenge here is to design a high gain PA under the low power consumption. In order to reduce the power consumption, each BJT has to be biased at a low base emitter voltage (V_{BE}). However, it leads to insufficient gain for the whole amplifier. To address this issue, we chose the multi-stage PA in our design. As shown in Fig.1, the first two stages of the PA are designed in the cascode format to increase the gain and isolation. The third and fourth common emitter (CE) stages provide more voltage headroom to drive the load. Besides, the Early effect of the hetero-junction bipolar transistor (HBT) helps to increase the gain for the CE stage.

PA is one of the most power hungry blocks in the RF front-end. In our TX chain, the mixer gain is designed only 3dB to satisfy the high linearity requirement. Our target is to achieve a high gain PA under the low DC current. The maximum PAE and the output power drops dramatically while decreasing the bias voltage of the BJT. We biased the output stage at a moderate voltage (0.85 V) to get the moderate output power and PAE. We also biased the first several stages at a low voltage (0.75V) to get the high gain PA at the low power consumption.
The HBT cut-off frequencies are \( f_r/f_{\text{max}} = 200/200 \text{ GHz} \), and the break-down voltage \( B V_{\text{CEO}} \) is 1.9V. Since the impedance seen from the base node is small, the voltage swing between collector and emitter is considerably designed higher than \( B V_{\text{CEO}} \). The voltage swing here is designed to be 3.6 V, which is close to the \( B V_{\text{CEO}} \). The transistors consists of two emitters, three bases and two collectors (CBEBEBC), which has better current capacity as well as the maximum power gain when compared to single-base device (CBE) and two-base device (CBEBC).

Impedance matching for the HBT transistors is achieved by using the conductor-backed coplanar waveguide (CBCPW) structures and metal-insulator-metal (MIM) capacitors. The CBCPW is design using top thick metal with the thickness of 2.81µm. The measured insertion loss of CBCPW at 60GHz is 0.23dB/mm. In order to increase the input matching bandwidth, a low-Q double-stub network is implemented by CBCPW to provide more design freedom. The \( Q_{\text{input-network}} \) is set to be <1.5. The output matching network transformed the 50Ω to the optimum impedance 36.7+j*19.1 by the load-pull simulation. To avoid oscillations, the small MIM capacitors with high self-resonant frequency (i.e., from 40 fF to 80 fF) is adopted.

Stability analysis is very important in the power amplifier design. The large signal s-parameter (LSSP) simulation in Agilent Design System (ADS) is used to analyse the large signal stability. LSSP simulation can be performed on nonlinear circuits and thus include nonlinear effects such as gain compression and variations in power levels. Compared with small signal s-parameter simulation, the LSSP generates the additional field which contains the power seen at each port for the respective LSSP port frequencies. Large signal stability of the proposed PA is simulated by driving the PA with the large signal input to make the PA output voltage swing close to its normal or peak value.

B. Wideband ESD Design

Diode is widely used for ESD protection at the I/O port. However, under very high frequency application, the parasitic capacitance associated with ESD diodes will degrade the RF performance of the core circuit seriously. We propose a new ultra wideband ESD protection structure without any diodes. This structure will not add parasitic capacitance to the power rail ESD clamp circuit. The merits of the proposed ESD protection structure are the compact size, low loss and wide RF bandwidth. The ESD circuit is designed by using the combination of CPW and CBCPW. The metal thickness of M1–M3 is 0.52 µm. The thickness of M6, M5 and M4 are 2.81
The V-band PA is implemented in SBC18H2 0.18-μm SiGe BiCMOS technology provided by Tower Jazz. Fig.3 shows the micrograph of the proposed ESD and PA. The core area of four-stage PA is 300μm×1040μm. The PA is unconditionally stable from DC to 90 GHz. Under the 2.4 V power supply, the total power consumption of four-stage PA is 100.3 mW.

The measured S-parameters of the four-stage PA are shown in Fig.4. It achieves a measured peak power gain of 20.8 dB under 1.8 V and 25.3 dB under 2.4 V at 67 GHz. The 3 dB bandwidth is 63-72 GHz. The S11<-10 dB bandwidth is from 40-75 GHz. Although the center frequency shifts up about 3 GHz (4.6%) after testing, the gain variation of the PA is still within 4 dB at two channels from 61.56 GHz to 65.88 GHz. Owing to the baseband VGA, the 4 dB gain variation can be easily compensated. The measured output impedance is

Fig. 4. Measured S-parameters of the four-stage PA.

Fig. 5. Measured |S11| and |S21| of the proposed ESD.

Fig. 6. Measured V-Band PA gain and PAE vs input power at 67 GHz.

III. EXPERIMENTAL RESULTS

The V-band PA is implemented in SBC18H2 0.18-μm SiGe BiCMOS technology provided by Tower Jazz. Fig.3 shows the micrograph of the proposed ESD and PA. The core area of four-stage PA is 300μm×1040μm. The PA is unconditionally stable from DC to 90 GHz. Under the 2.4 V power supply, the total power consumption of four-stage PA is 100.3 mW.

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Fig. 7. CPW ESD TLP measurement results (PS mode)

Fig. 8. CPW ESD TLP measurement results (NS mode)
mismatched to 50Ω. This is because the output matching networks are optimized for maximum output power instead of maximum gain as input matching networks. The measured [22] fits well with the load-pull simulation result.

The measured [SI] and [S2] of standalone ESD are shown in Fig.5. The [S11] is lower than -10 dB from 17 to 110 GHz with on-wafer measurement. The insertion loss including the two GSG pads loss is lower than 1dB from 17 to 88 GHz.

Fig.6 shows the measured PA gain and PAE versus input power under two different bias conditions. The output-referred 1dB compression point of the four-stage PA is about 5.6 dBm and the Psat is 8.4 dBm under 2.4 V supply. The peak PAE for four-stage PA is 6.3%. The target of our project is to design a 60GHz transceiver with the lowest power consumption. The Psat and PAE are not optimized to the best due to the low power and high gain trade-off. The total power consumption of four-stage PA is 51.48 mW under 1.8V supply and 100.3 mW under 2.4V supply respectively. Since the PA output signal is AC coupled to the ESD and the PA is biased at the class-A condition, the power consumption of PA without ESD is almost the same with PA with ESD. We can estimate that the maximum PAE degradation is 2.4 % due to the 1dB ESD insertion loss.

To investigate the turn-on behavior and the I-V characteristics in high-current regions of the wideband ESD, the model 4002 transmission line pulsing (TLP) system with a 10-ns rise time and a 100-ns pulse width is used [9]. Fig.7 shows CPW ESD PS-mode (Positive ESD stresses at input port, and VSS is grounded). The transmission line shunt stub works as a resistor under the TLP stress with the resistance in the range 0.5–0.6 Ω. The voltage is clamped below 6 V even under the 10A ESD current. Fig.8 shows the CPW ESD NS-mode (Positive ESD stresses at VSS, and input port is grounded). The TLP measurement result of the NS mode has a similar performance with PS mode, since the structure of ground shunt stub is passive reciprocal network.

Table II summarizes performance of design PA together with PA of the prior art.

<table>
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<th>Ref</th>
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<th>Freq (GHz)</th>
<th>Gain (dB)</th>
<th>OP1dB (dBm)</th>
<th>Psat (dBm)</th>
<th>PAE (%)</th>
<th>Pdc (mW)</th>
<th>Vdd (V)</th>
<th>Gain/Pdc</th>
<th>ESD</th>
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<tr>
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<td>5.6</td>
<td>8.4</td>
<td>6.3</td>
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<td>2.4</td>
<td>0.253</td>
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<td>15.5</td>
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IV. Conclusion

Low-power high-gain V-band PA using 0.18-μm SiGe BiCMOS process has been designed and verified. The PA demonstrates lowest power consumption and good gain among the reported SiGe PA. Simultaneously, a novel wideband ESD protection circuit with low insertion loss and compact size is also introduced into our designed PA. It is clear that the proposed designs are suitable for the low power consumption mm-wave transceivers in mobile applications.

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REFERENCES